

# Compal Confidential

## QAL51 MB Schematic Document

### LA-7871P

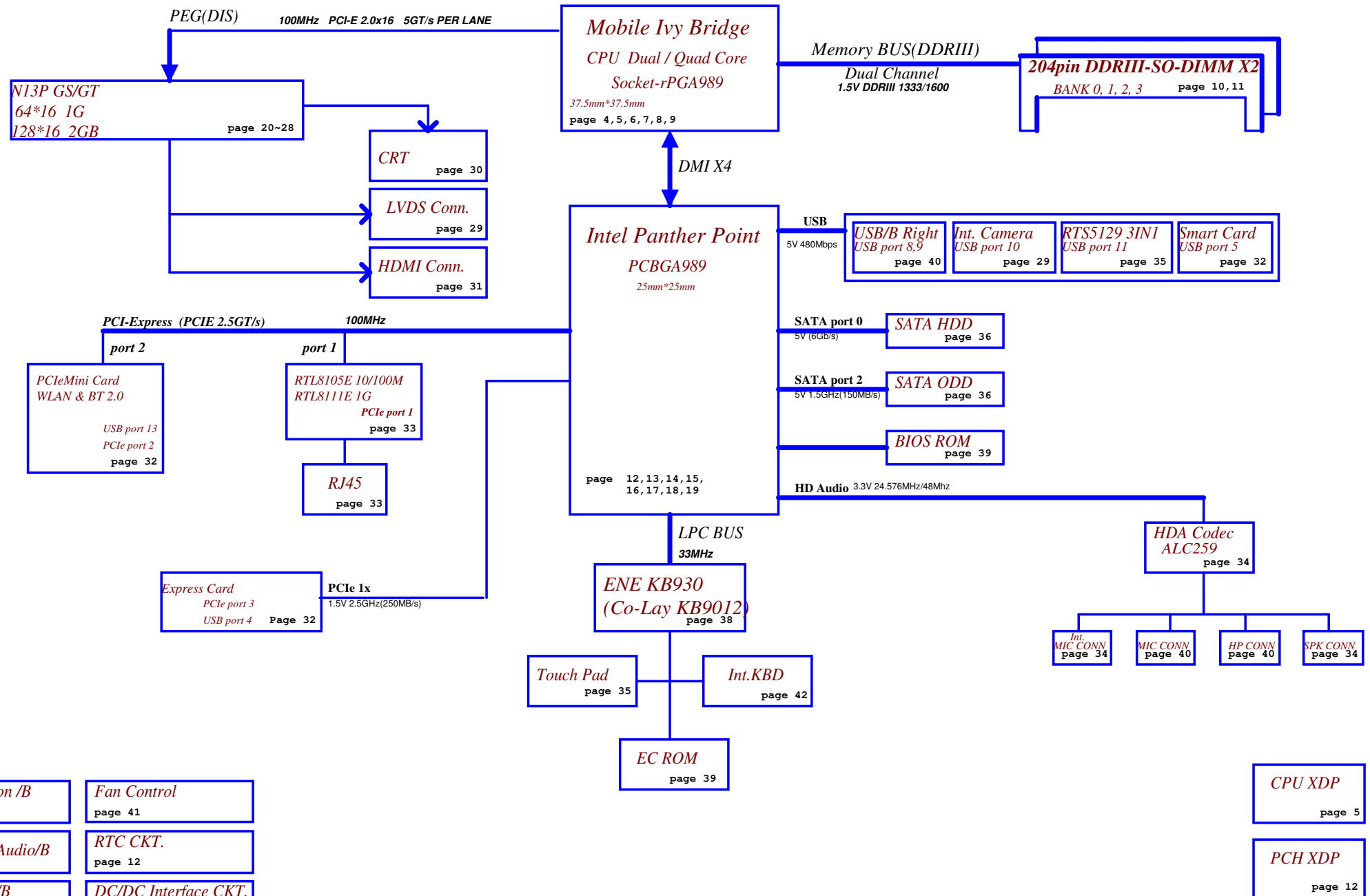
Intel Ivy Bridge / Panther Point

Discrete : N13P-GS / N13P-GT

Rev: 1.0

2012.02.29

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2012/12/31	Title <b>Cover Sheet</b>	
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title <b>Chief River-Block Diagram</b>	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	QAL31 / LP
2	QAL31 / GT
3	
4	QAL50
5	QAL51 / GS
6	
7	QAL51 / GT

PCH

USB PORT#	DESTINATION
0	USB2/3 (Left Hand side front)
1	USB2/3 (Left Hand side back)
2	None
3	None
4	USB2 (Right Hand side front)
5	Smart CARD
6	None
7	None
8	EXPRESS CARD
9	USB2 (Right Hand side back)
10	CAMERA
11	Card Reader
12	Finger Print
13	BT Comb

SMBUS Control Table

	SOURCE	MIINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	VGA Int. Thermal 0x9A	JXDP1 JXDP2
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V	X
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V	X	V
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	X	V	X

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None

OPTIMUS: XDP@/D@

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	Express Card	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

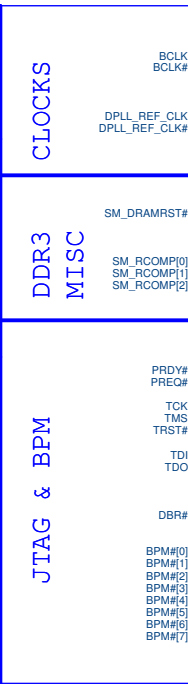
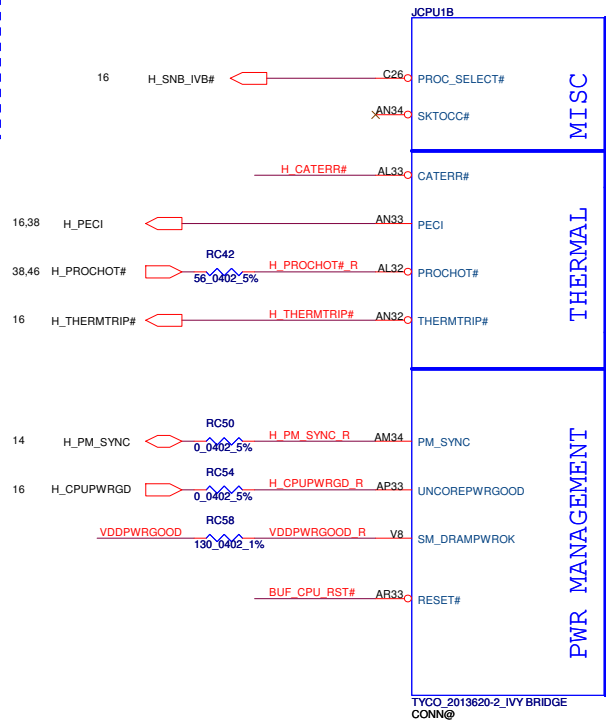
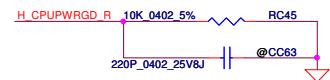
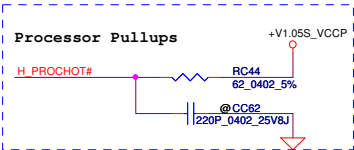
 : means Analog Ground

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

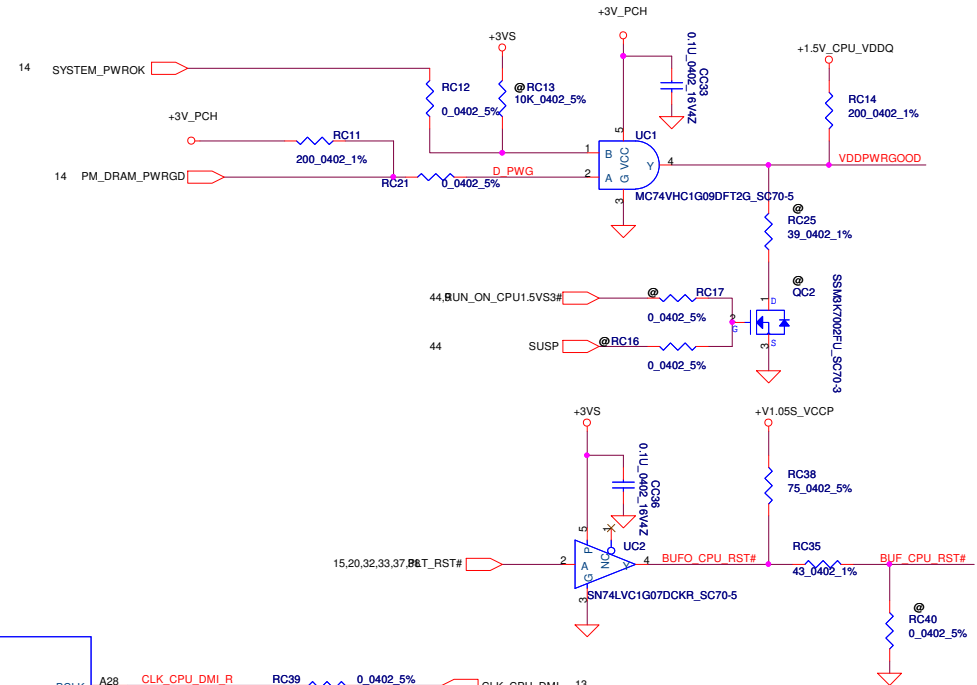
PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	Express Card
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

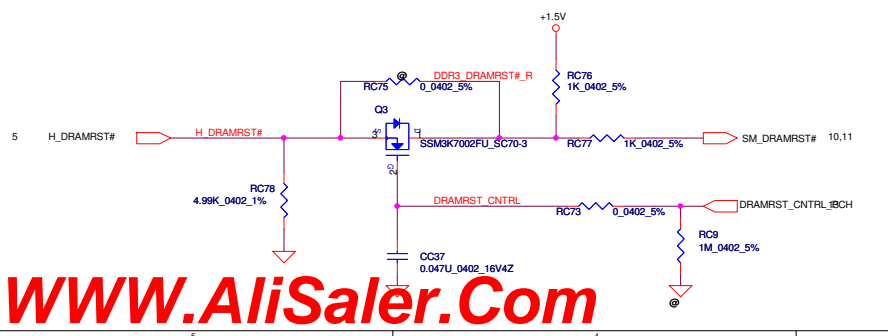
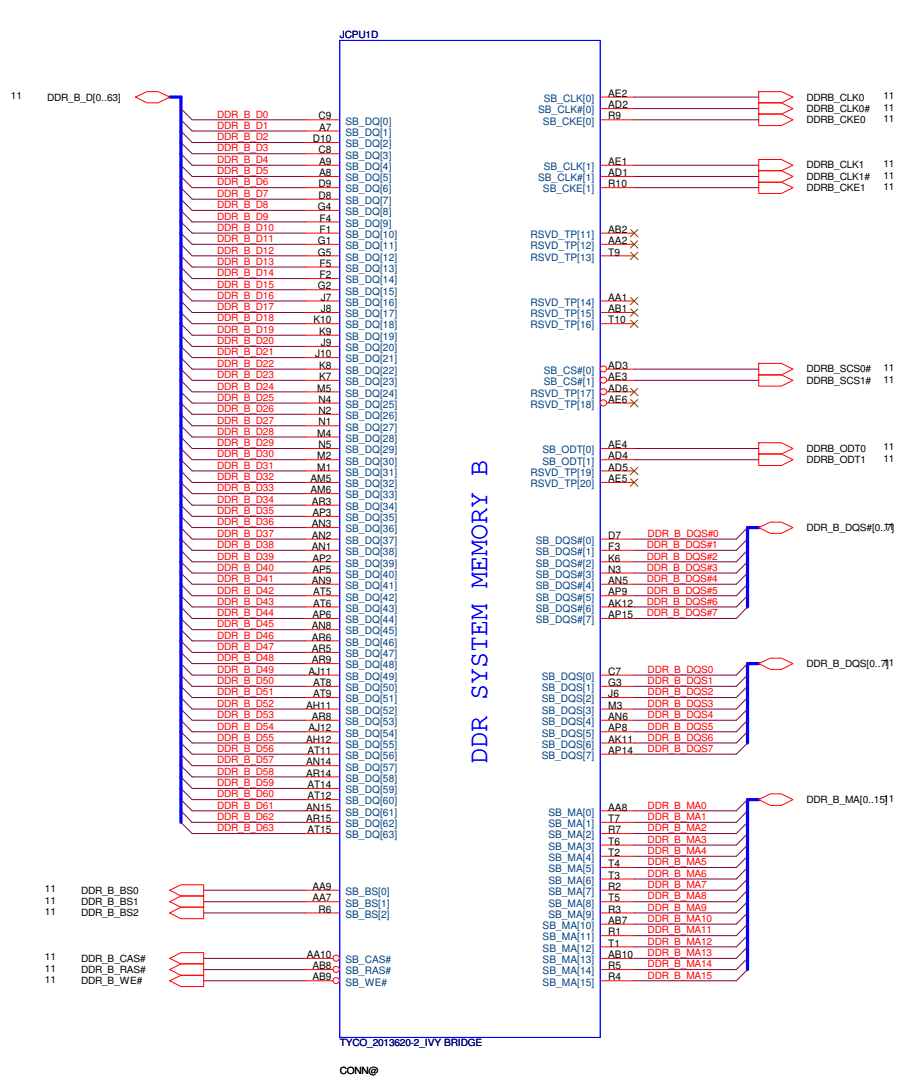
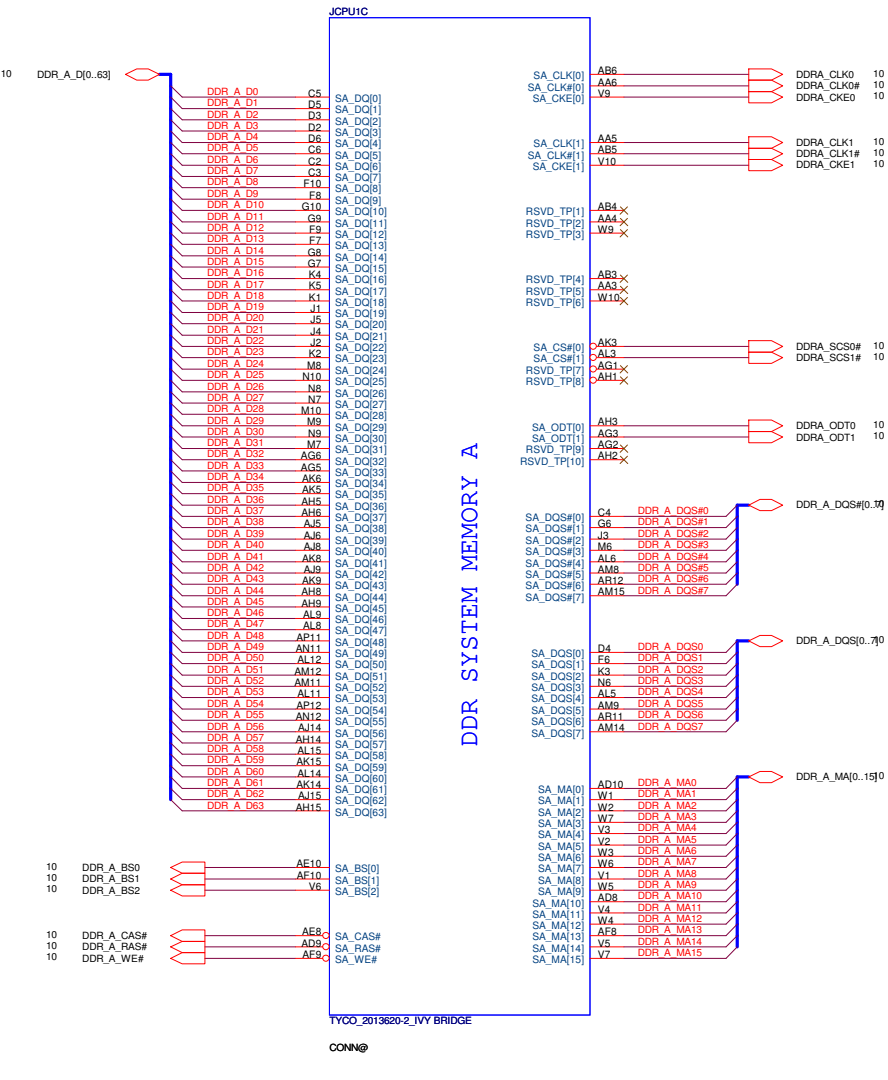
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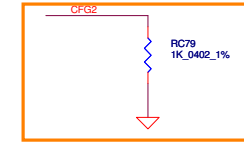
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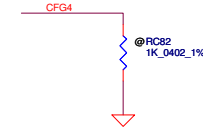
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Title		PROCESSOR(3/6) DDRIII			
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## CFG Straps for Processor



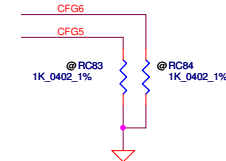
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--



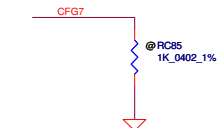
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
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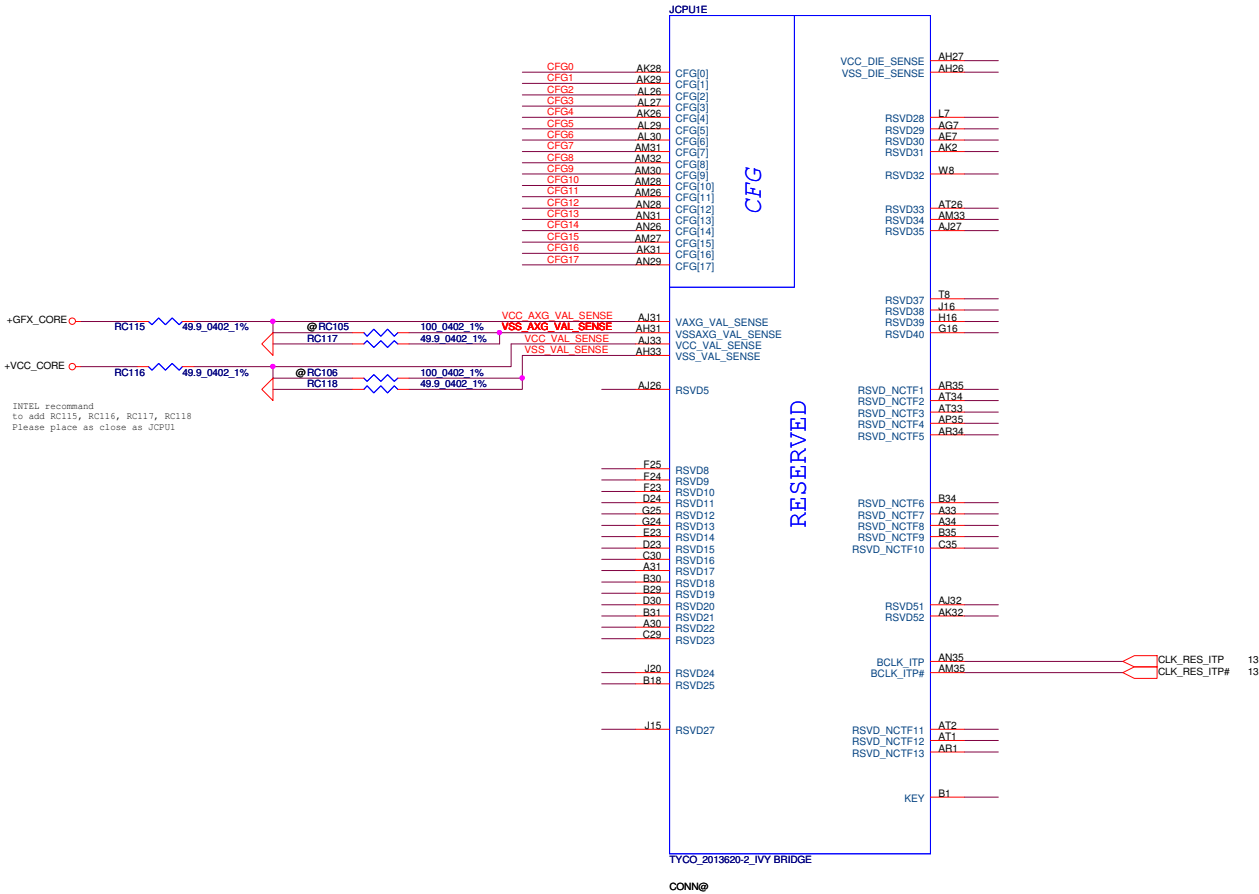
PCIe Port Bifurcation Straps

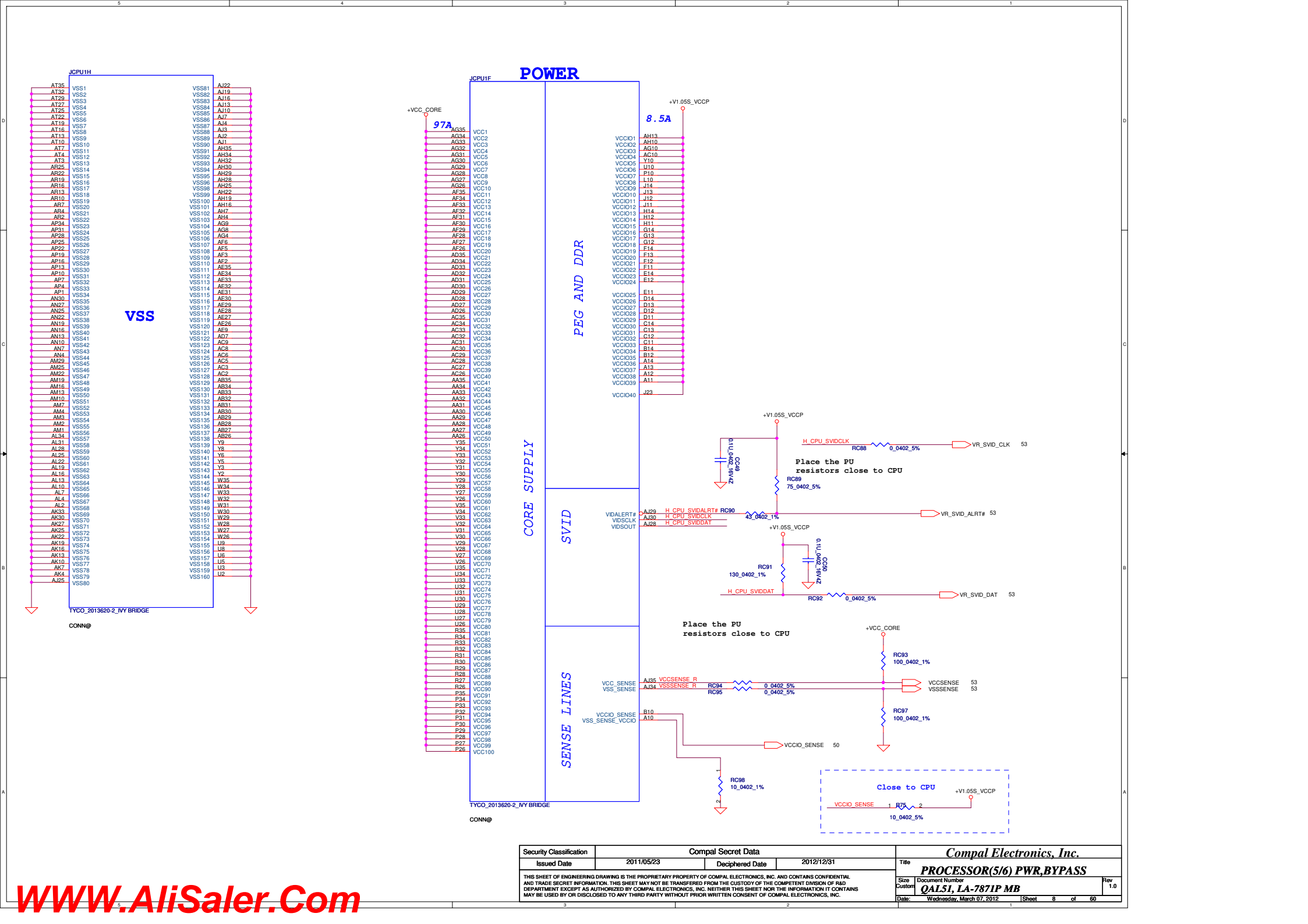
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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PEG DEFER TRAINING

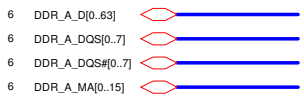
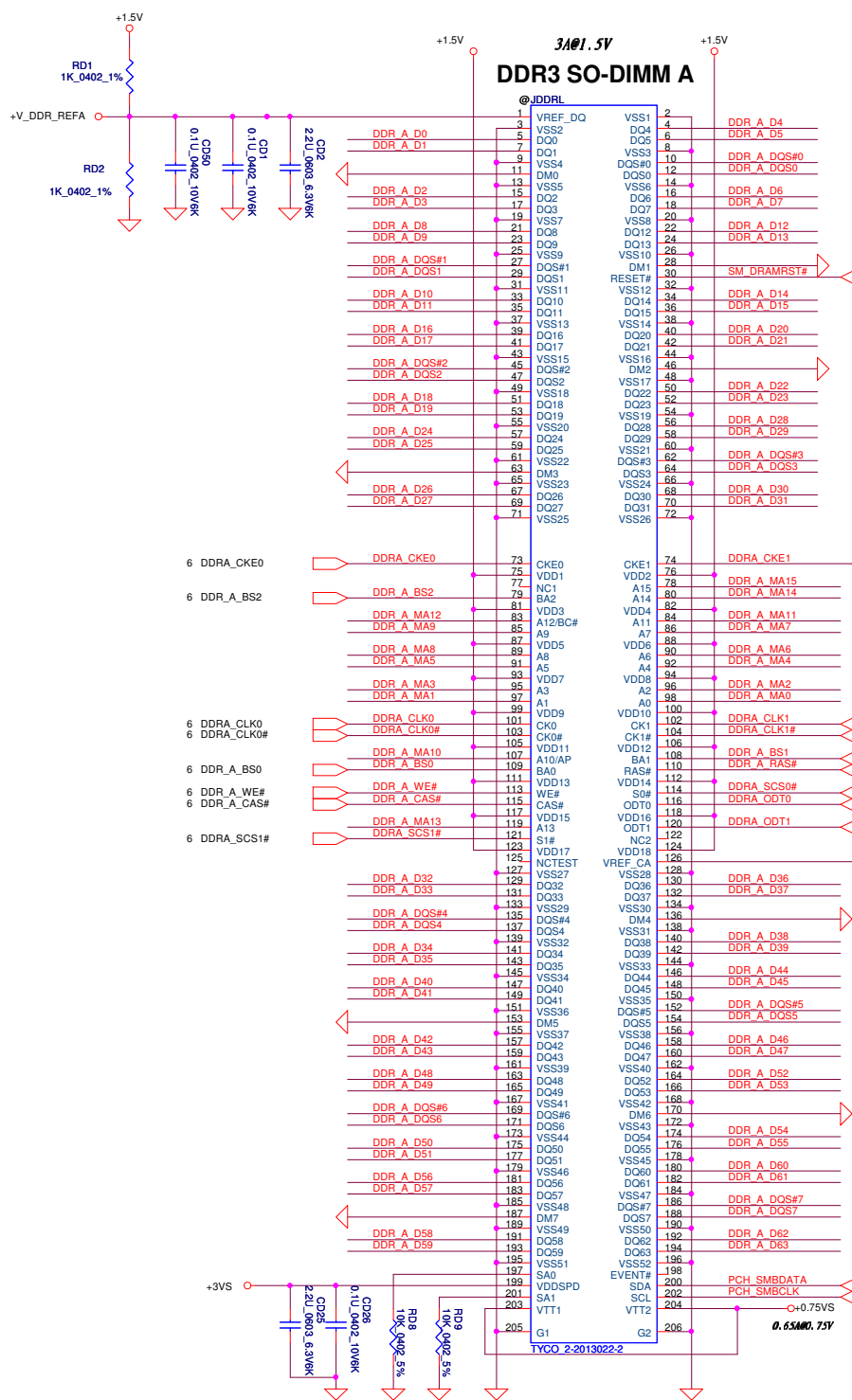
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training
------	---











SM\_DRAMRST#11.6

DDR\_A\_CKE1

DDR\_A\_CLK1

DDR\_A\_BS1

DDR\_A\_SC0#

DDR\_A\_ODT0

DDR\_A\_ODT1

DDR\_A\_D36

DDR\_A\_D37

DDR\_A\_D38

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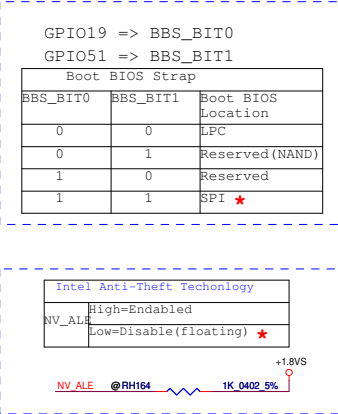
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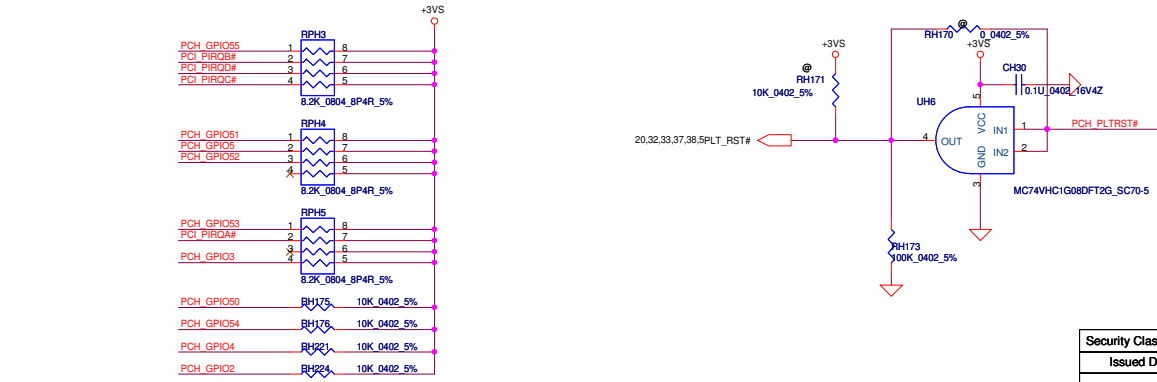
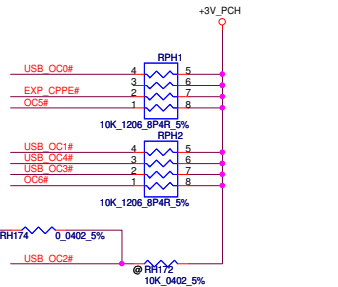




GPI019 => BBS\_BIT0  
GPI051 => BBS\_BIT1

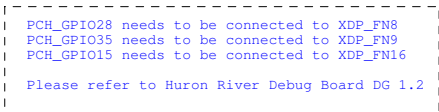
Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Technology	
NV_ALF	High=Enabled
	Low=Disable(floating) ★



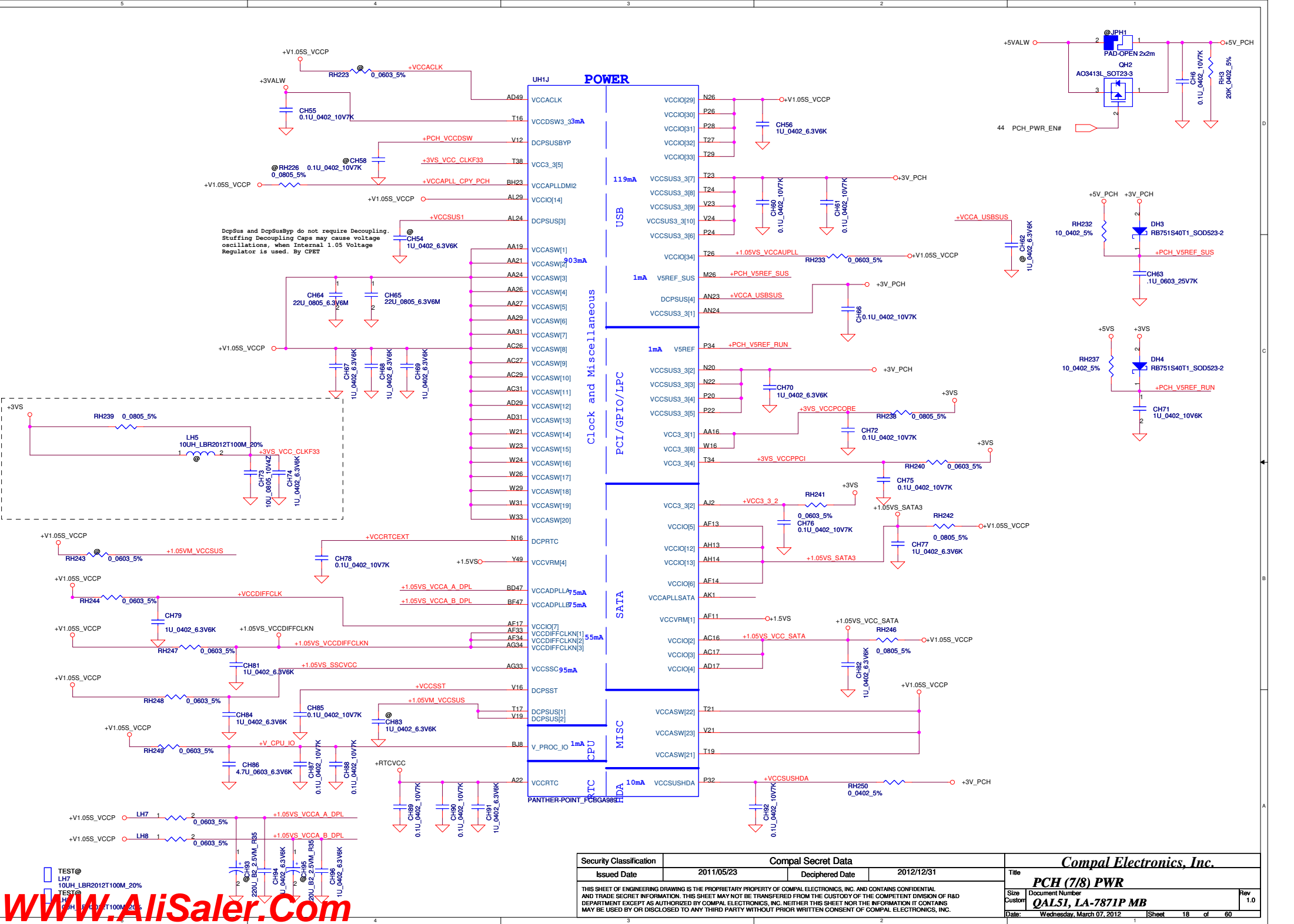
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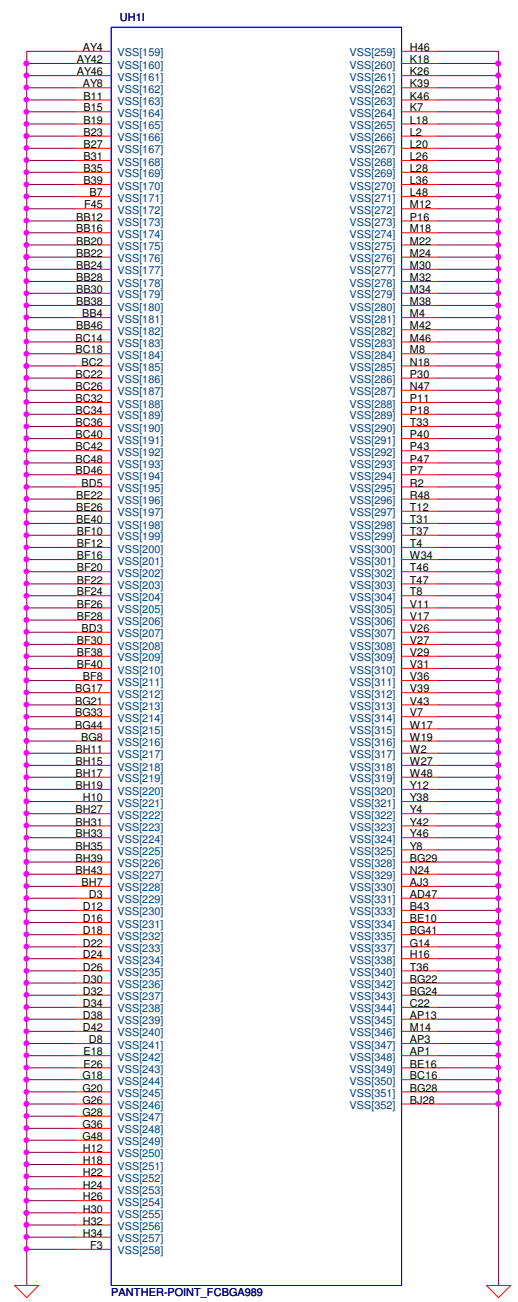
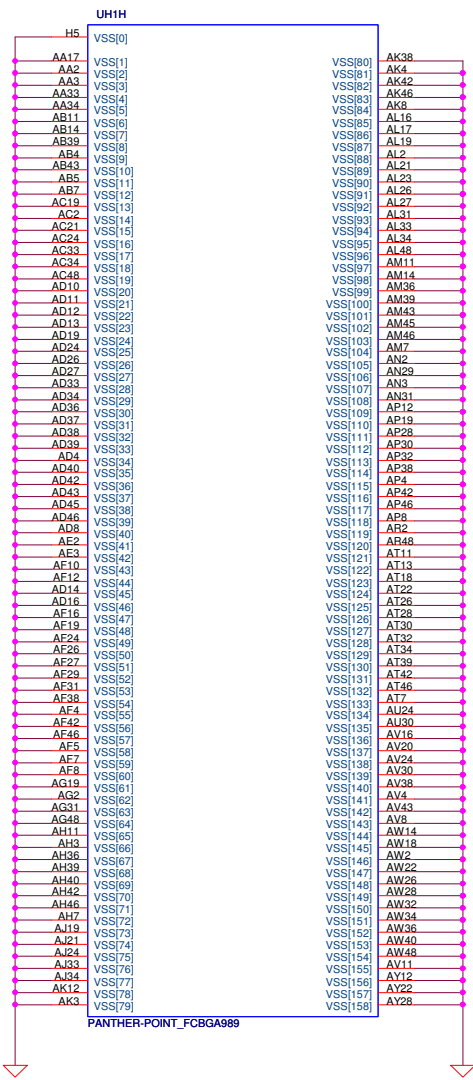






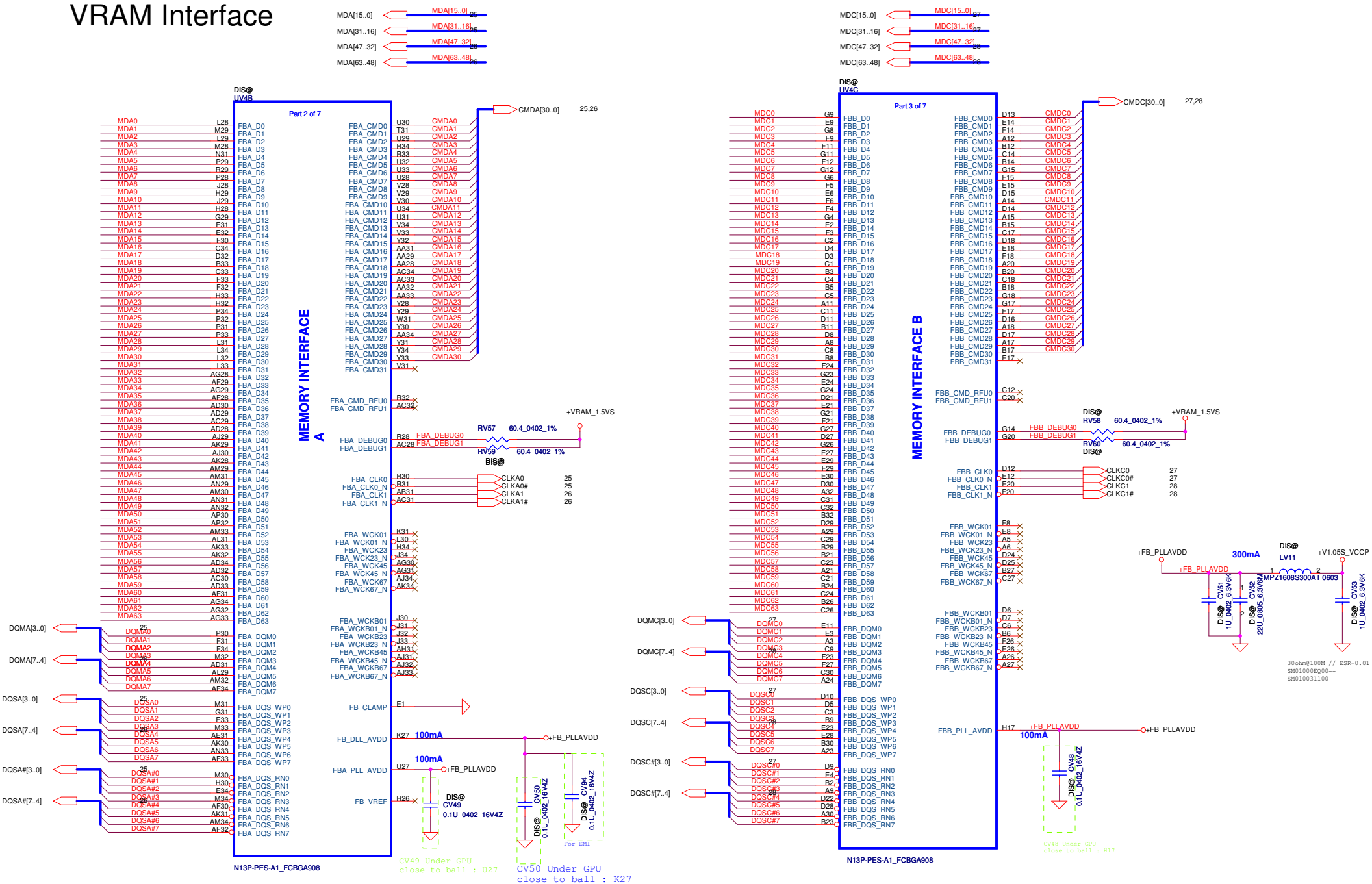
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Compal Electronics, Inc.	
PCH (7/8) PWR	
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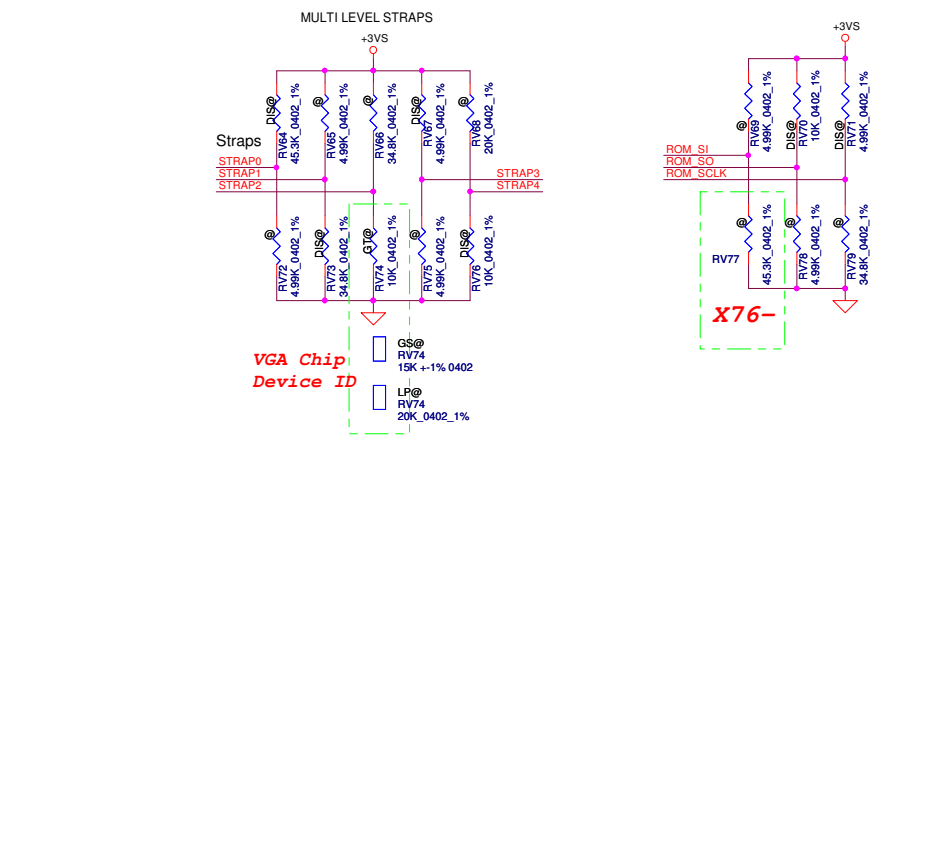
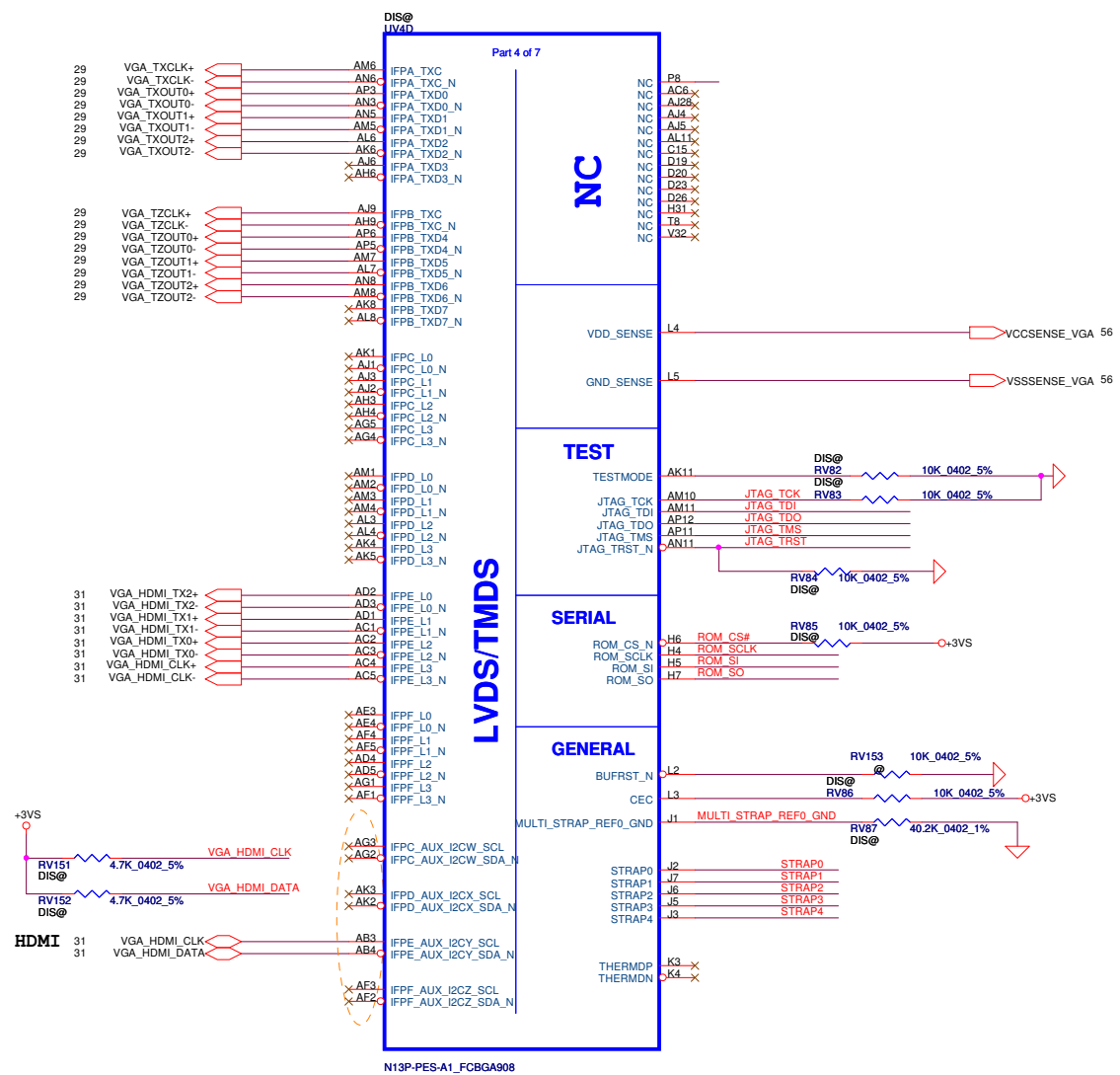




## VRAM Interface



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For N13P-GS/GT/LP strap table											
GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO00	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K
N13P-GT	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO00	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K
N13P-LP	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO00	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K

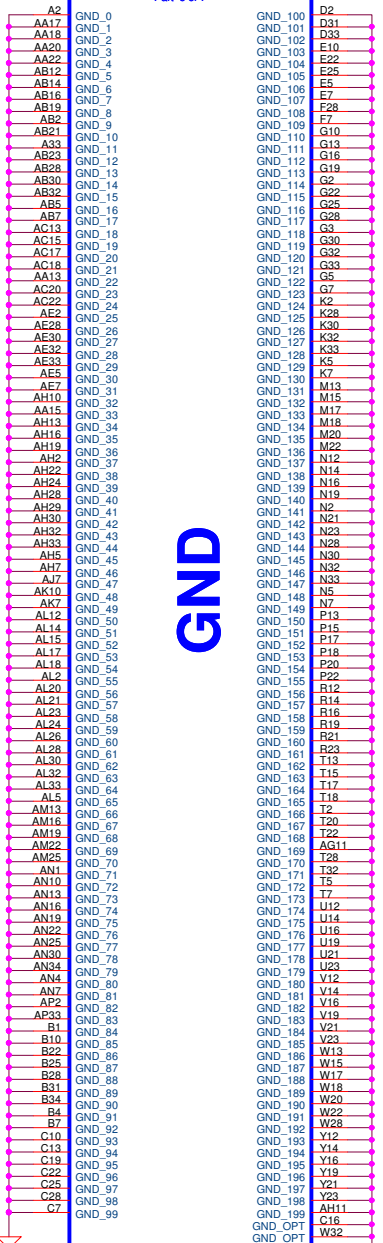




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UV4F

Part 6 of 7



N13P-PES-A1\_FCBGA908

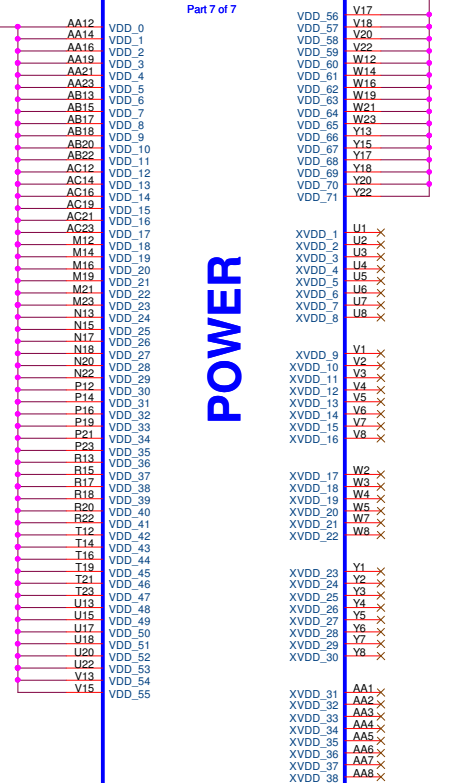
DIS@

+VGA\_CORE

60A

UV4G

Part 7 of 7



N13P-PES-A1\_FCBGA908

DIS@

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				Size		Document Number		Rev	
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				Date:					
				Wednesday, March 07, 2012					
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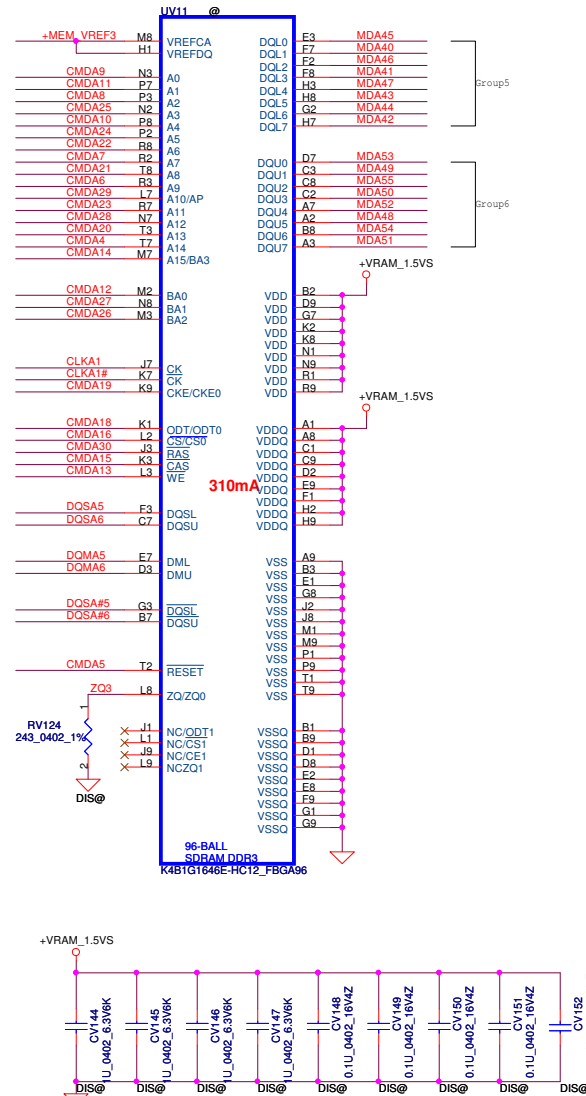
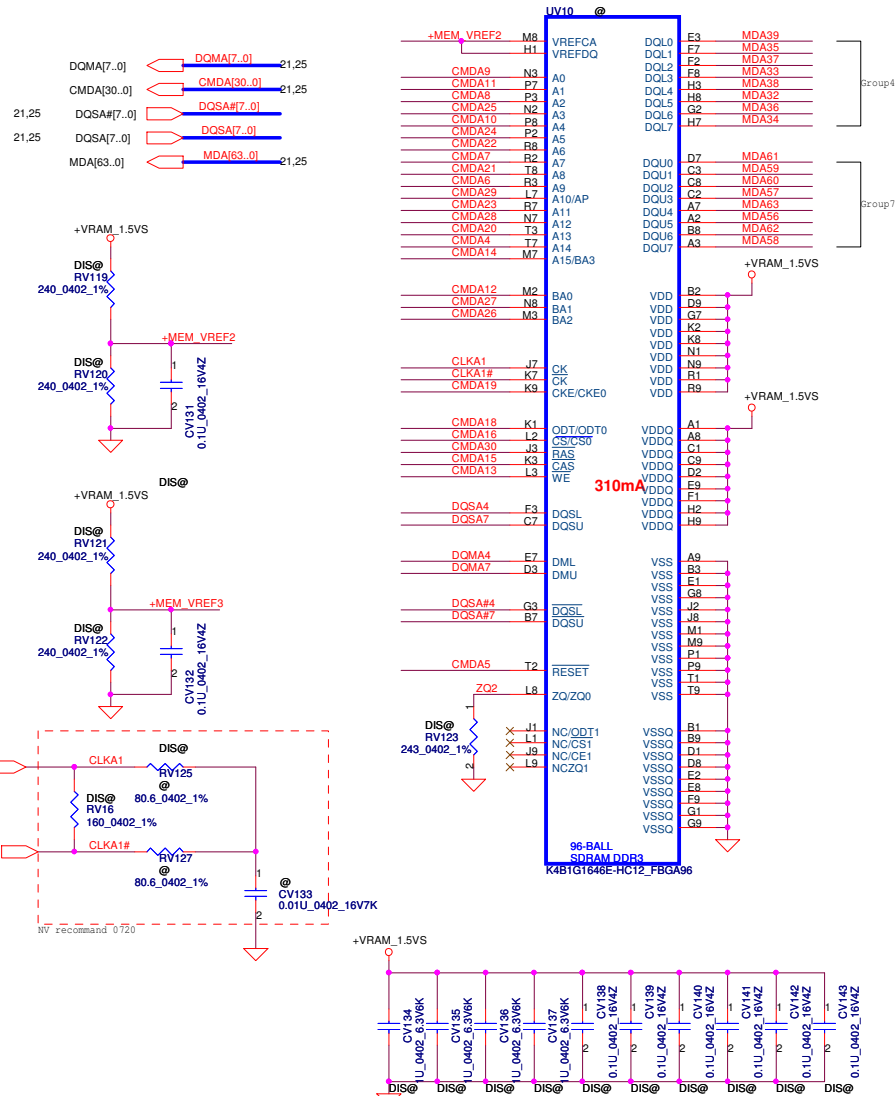


**64Mx16 DDR3 \*8==>1GB**  
**128Mx16 DDR3 \*8==>2GB**

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

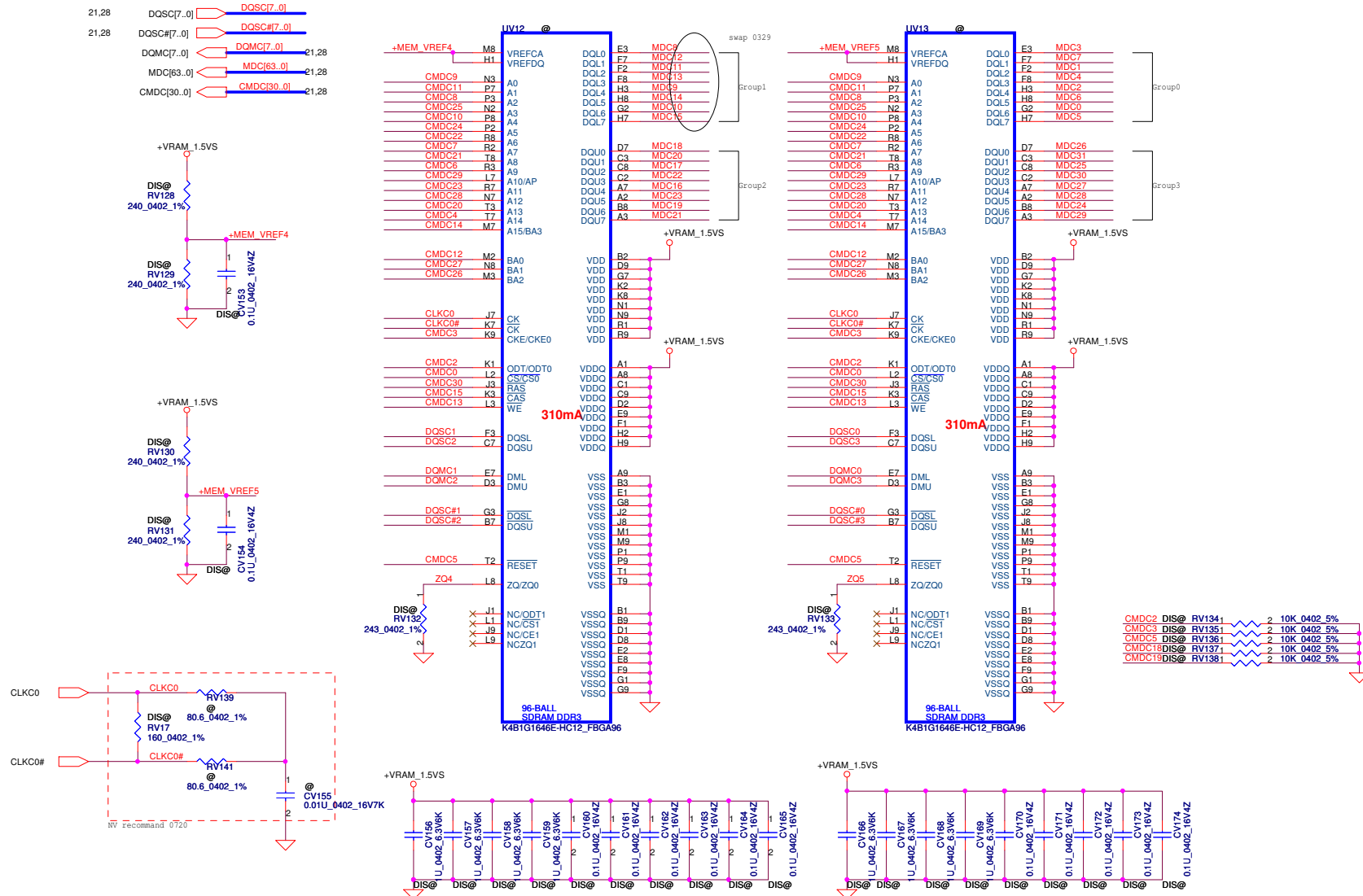
128Mx16 DDR3 \*8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

64Mx16 DDR3 \*8==>1GB  
128Mx16 DDR3 \*8==>2GB



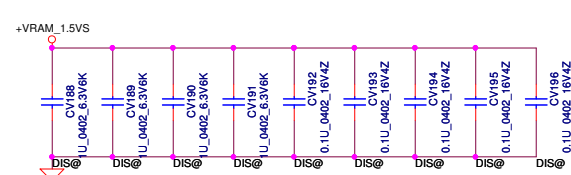
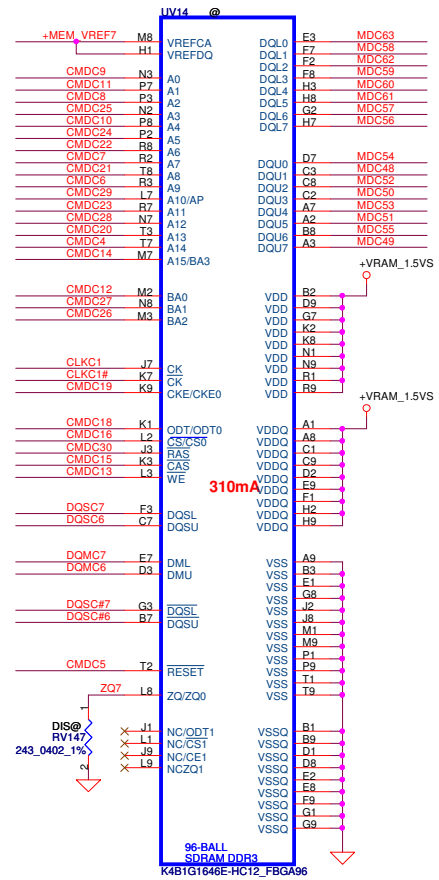
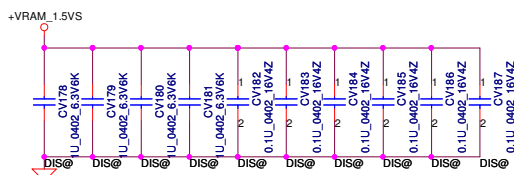
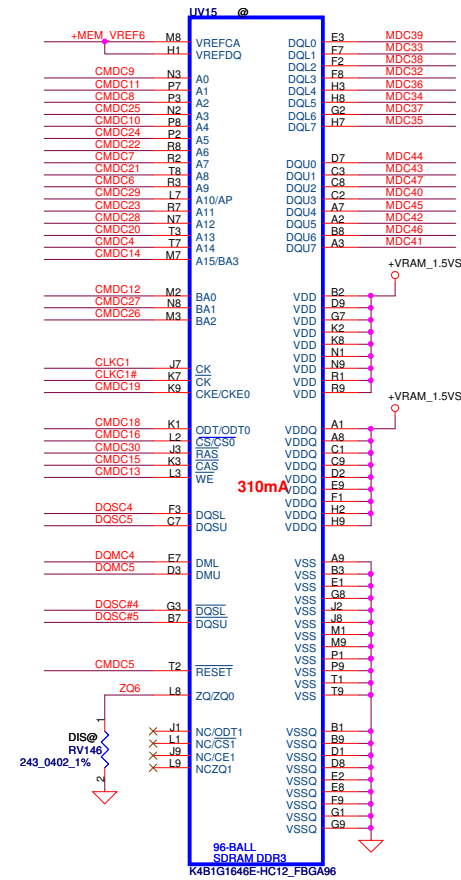
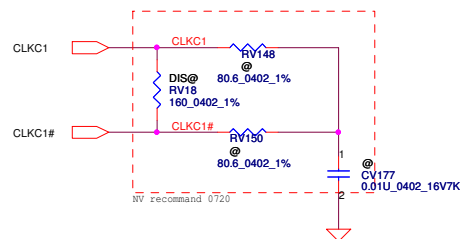
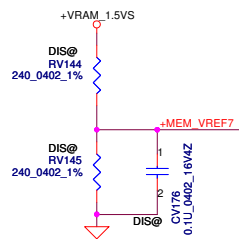
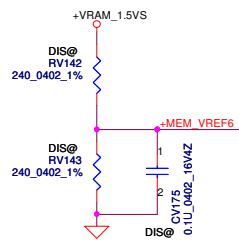
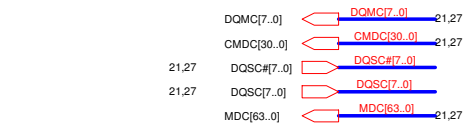
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

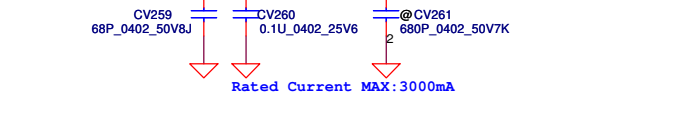
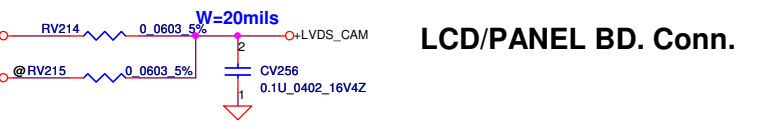
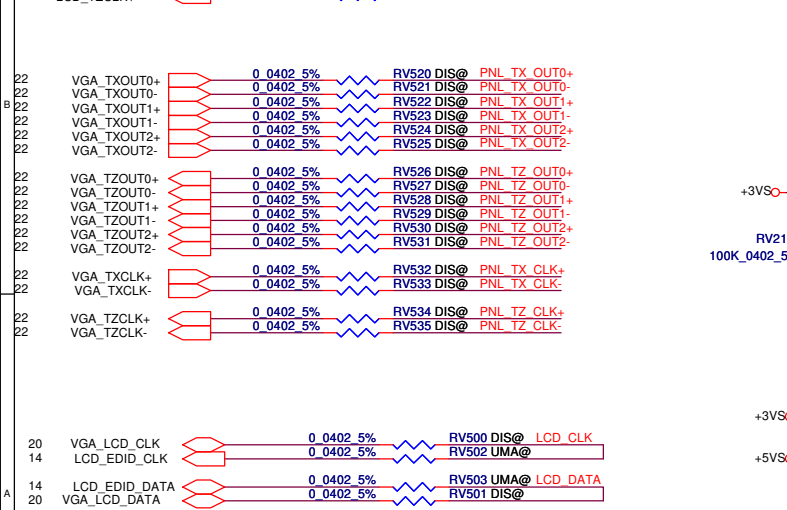
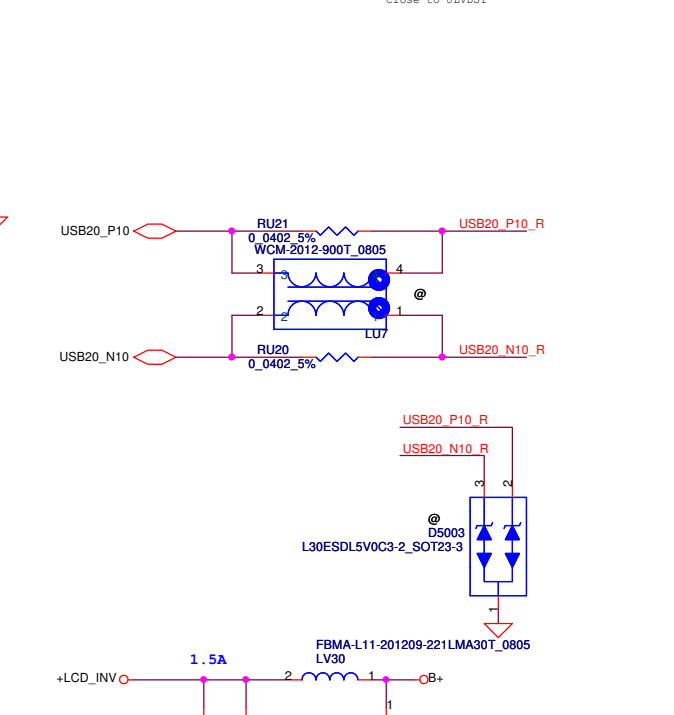
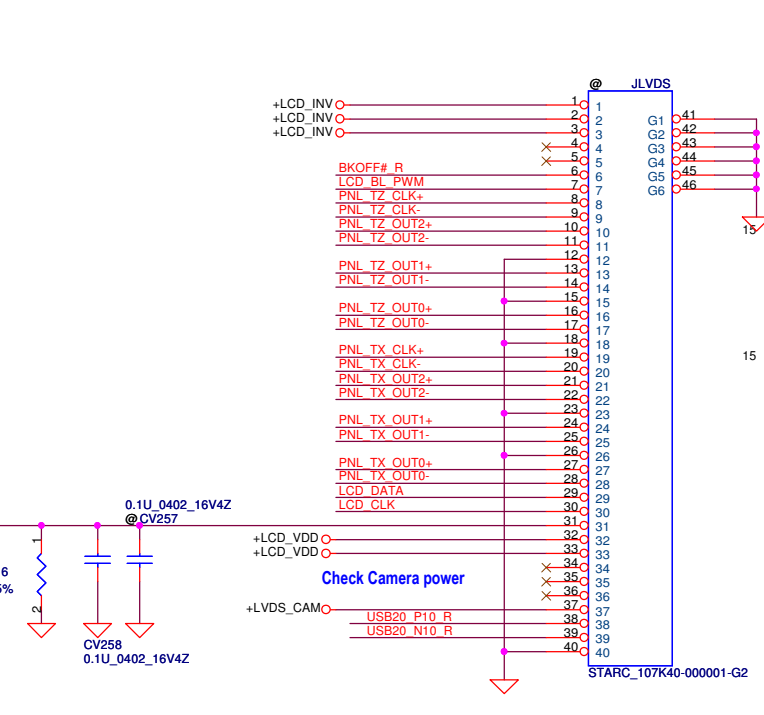
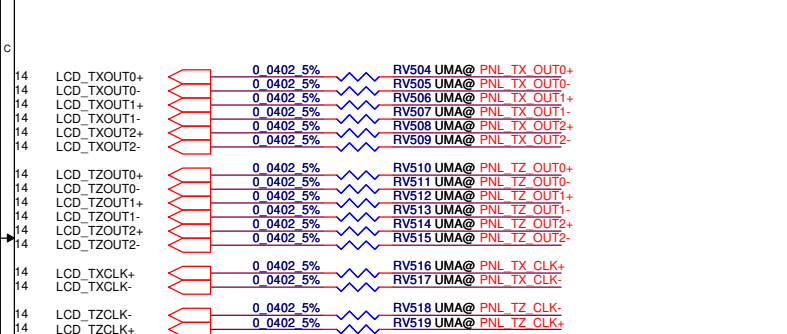
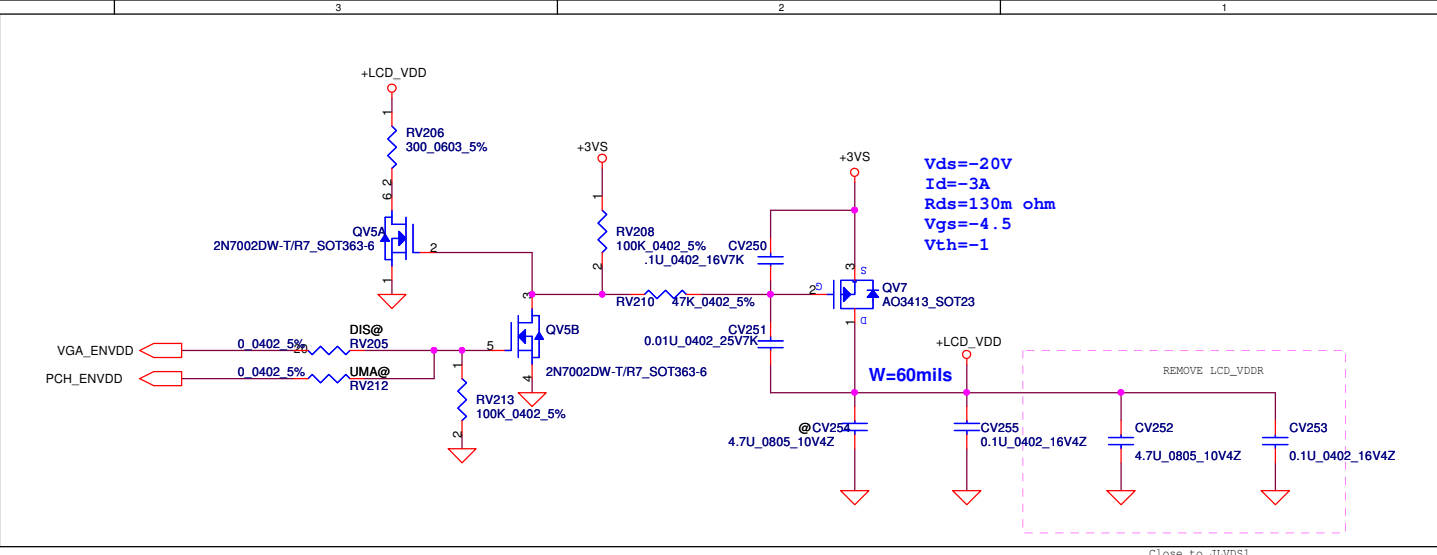
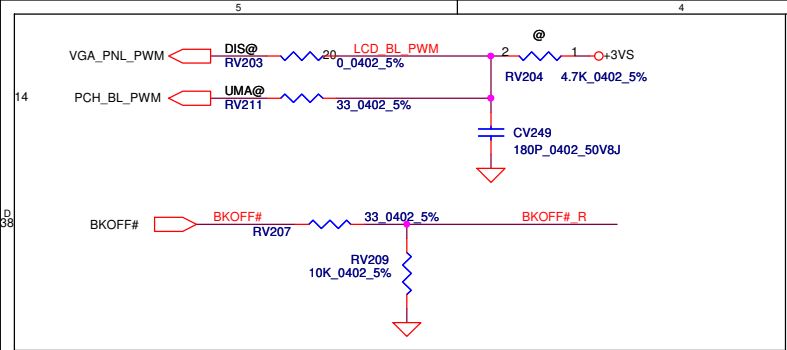
128Mx16 DDR3 \*8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

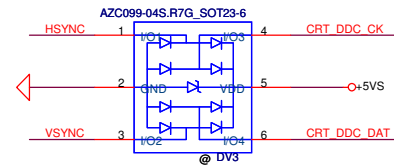
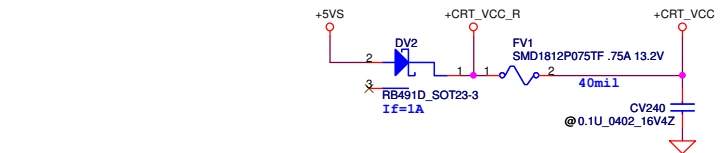
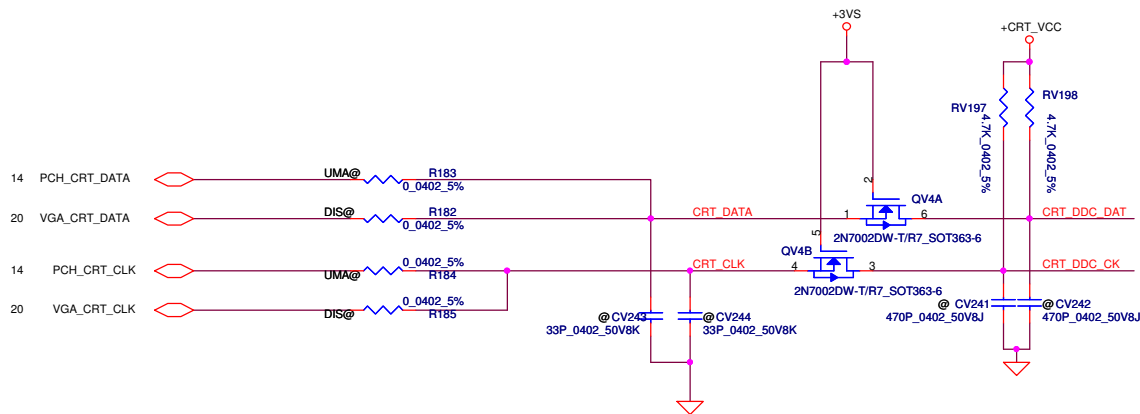
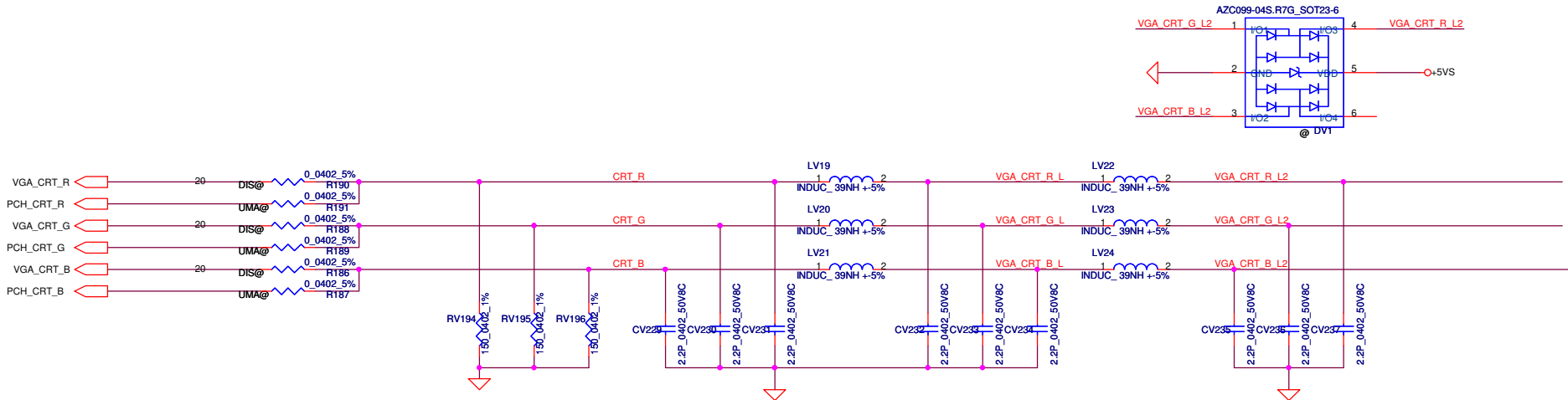
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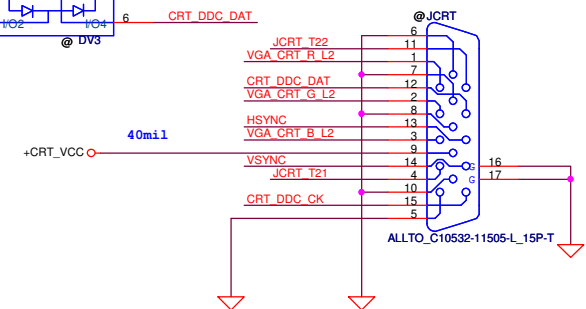
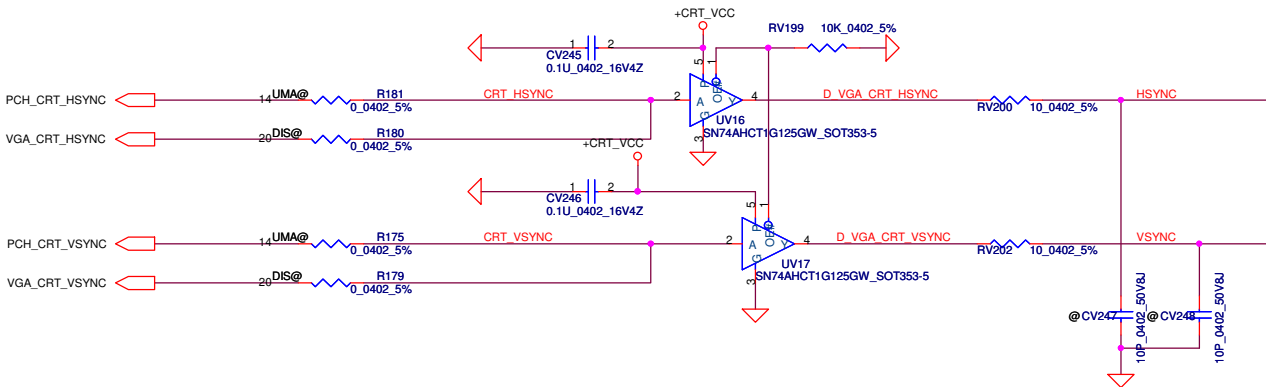


## LCD/PANEL BD. Conn.

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## CRT CONNECTOR

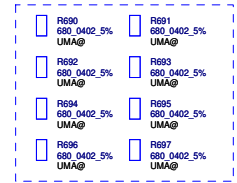
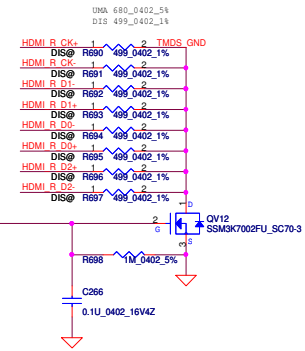
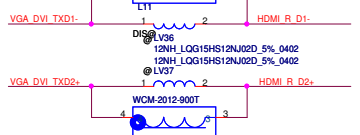
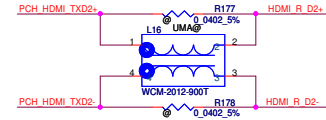
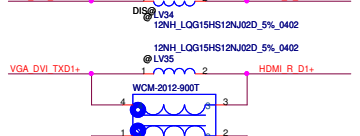
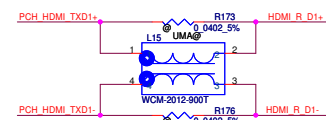
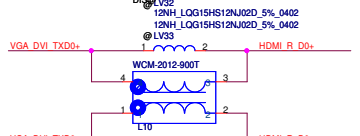
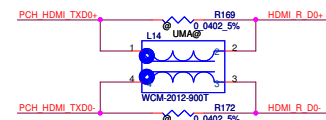
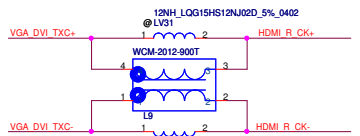
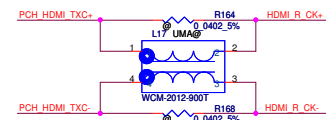
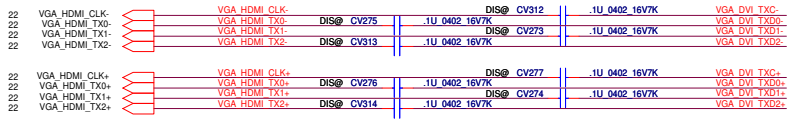
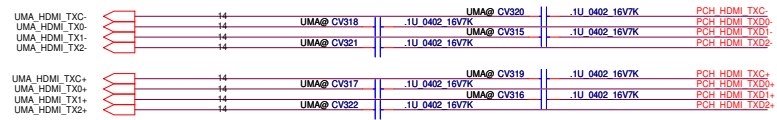
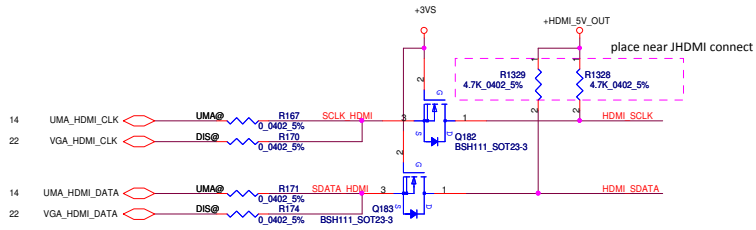
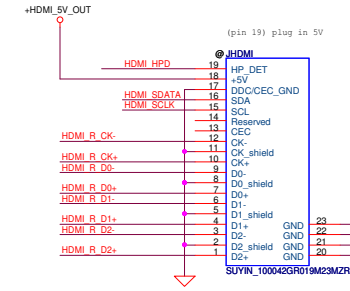
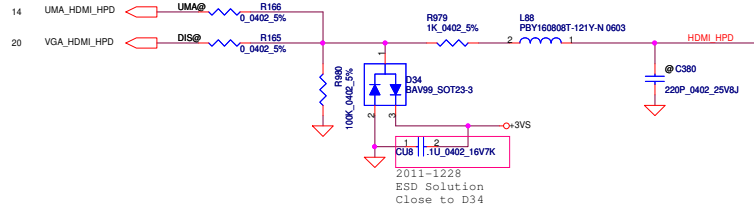
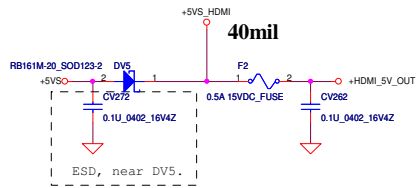


Close to CRT Connector

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										Wednesday, March 07, 2012	
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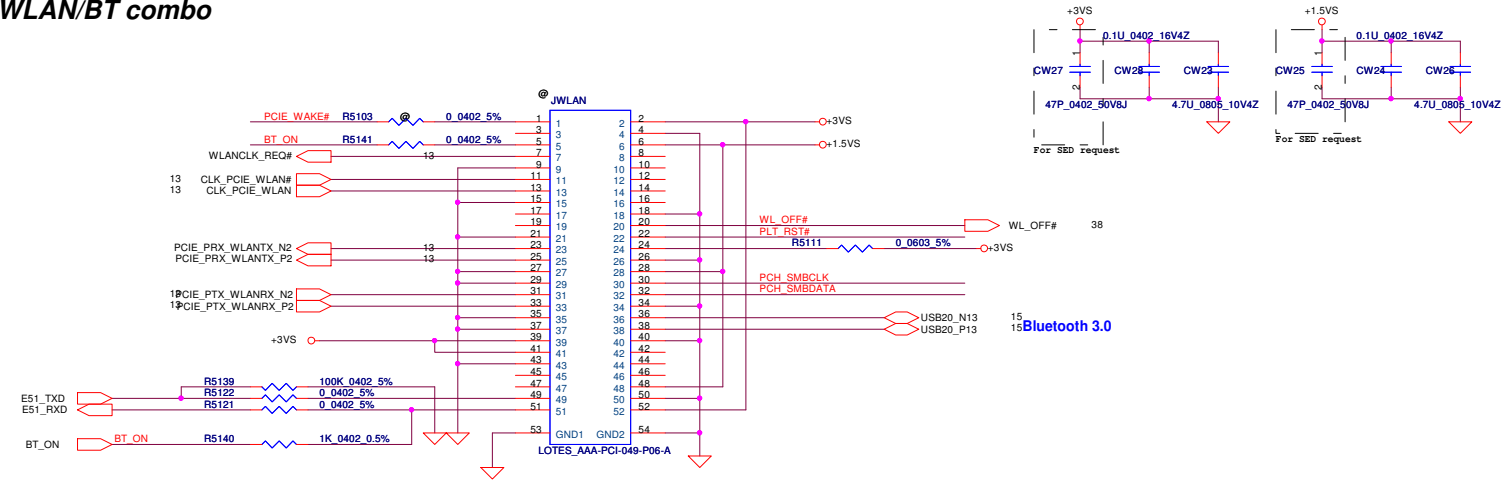
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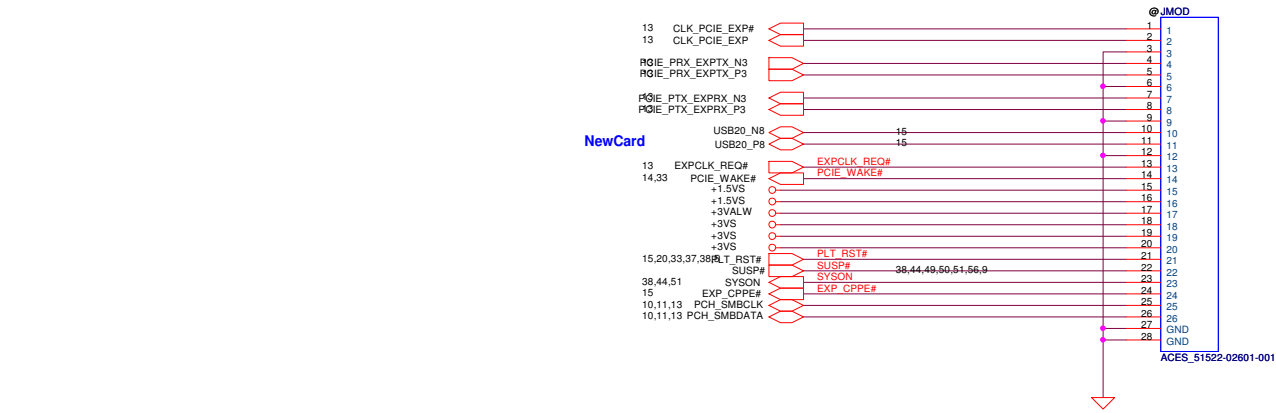
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					Size	Document Number	Rev
					C	QAL51_LA-7871P MB	1.0
Date:					Wednesday, March 07, 2012		
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WWW.AliSaler.Com

WLAN/BT combo



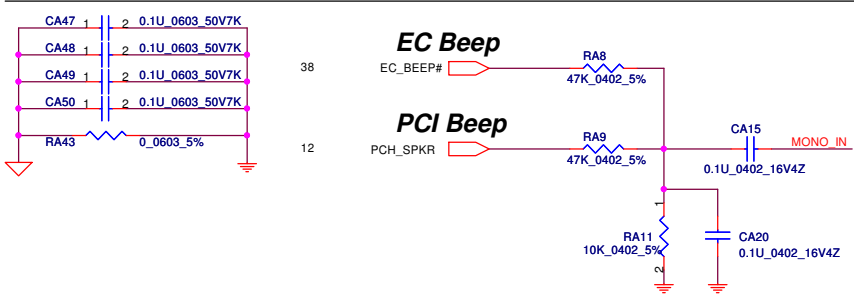
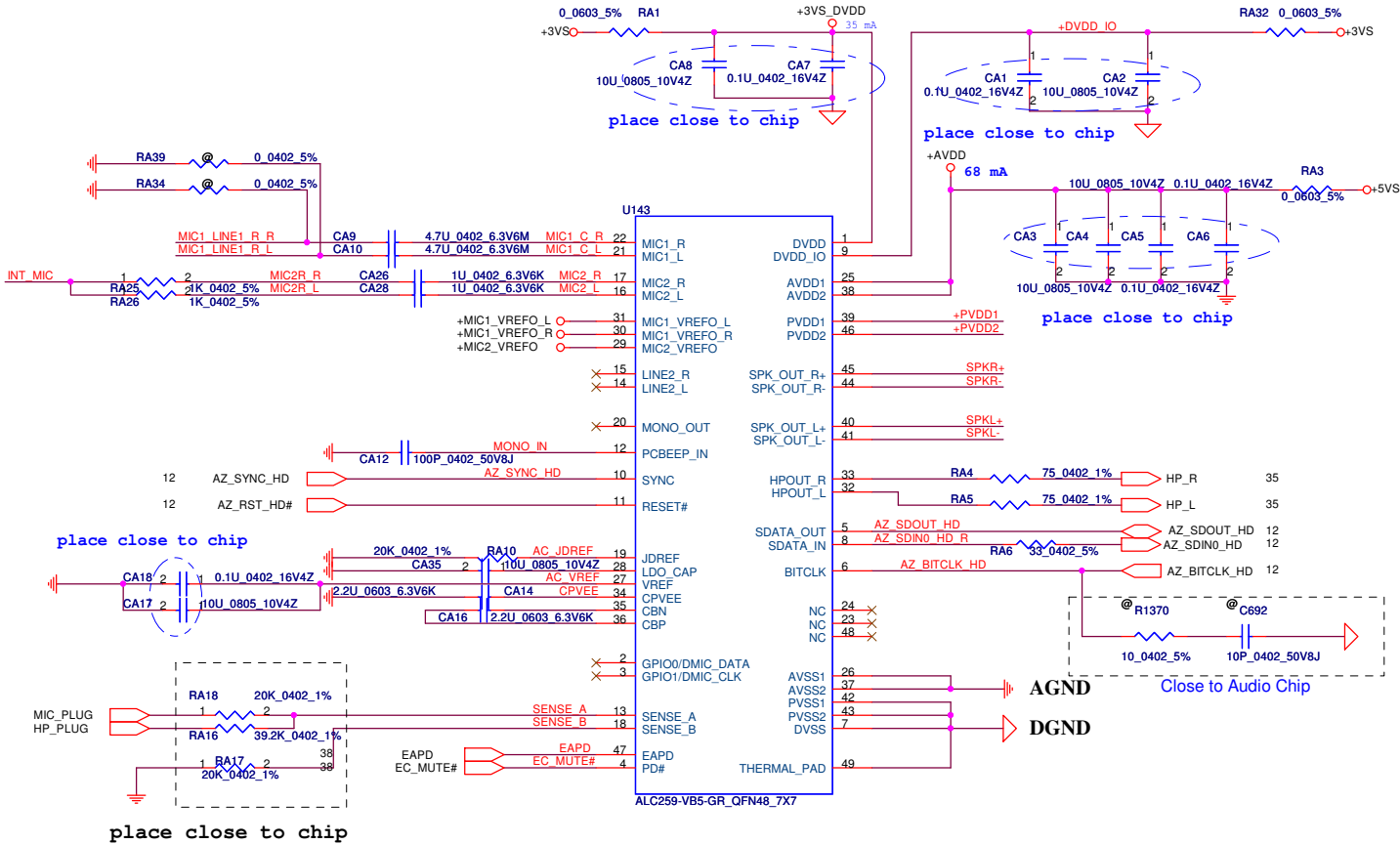
NewCard & Smart Card



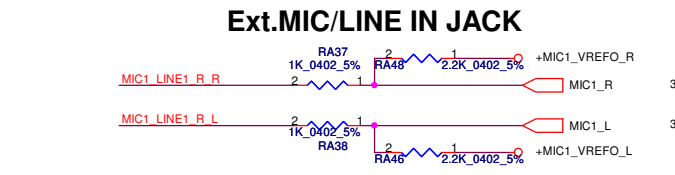
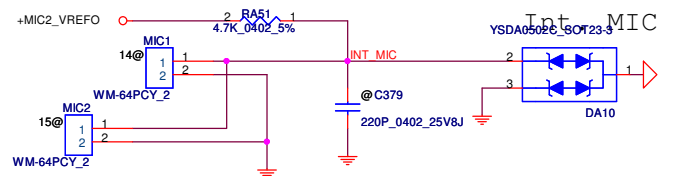
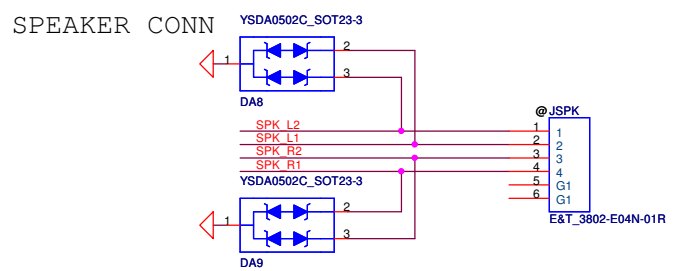
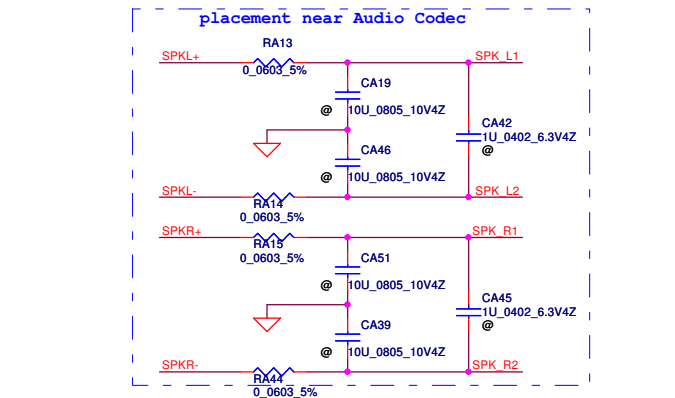
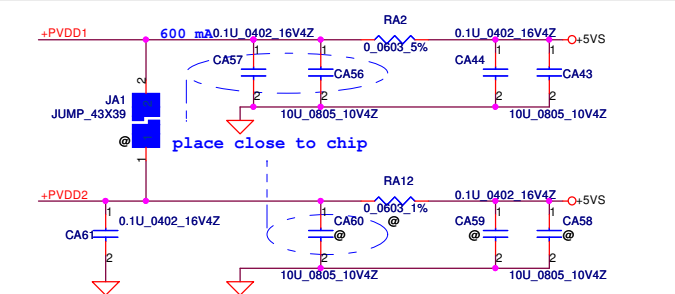
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	WLAN/ WWAN/ m-SATA
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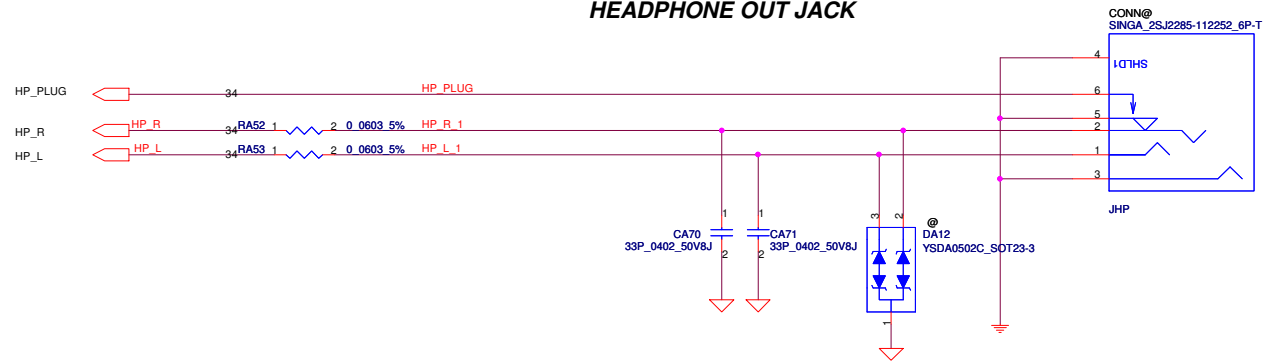


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

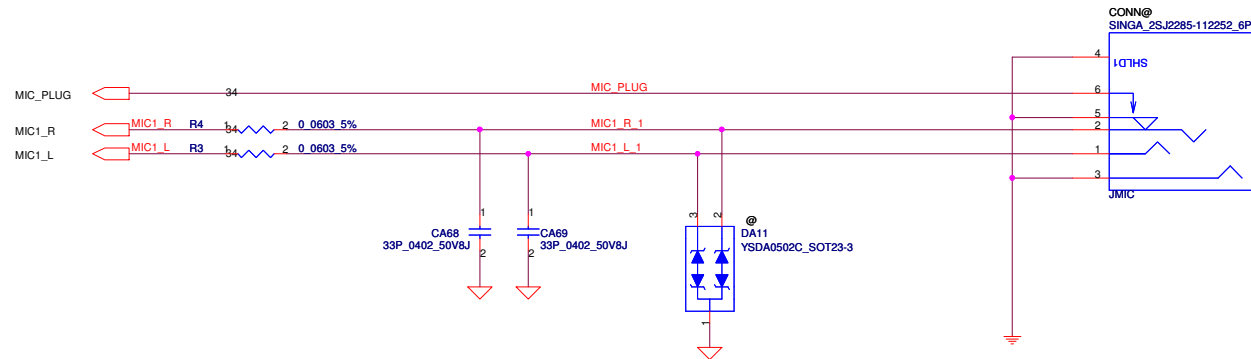


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				Size	Document Number
				QAL51, LA-7871P MB	
				Date	Wednesday, March 07, 2012
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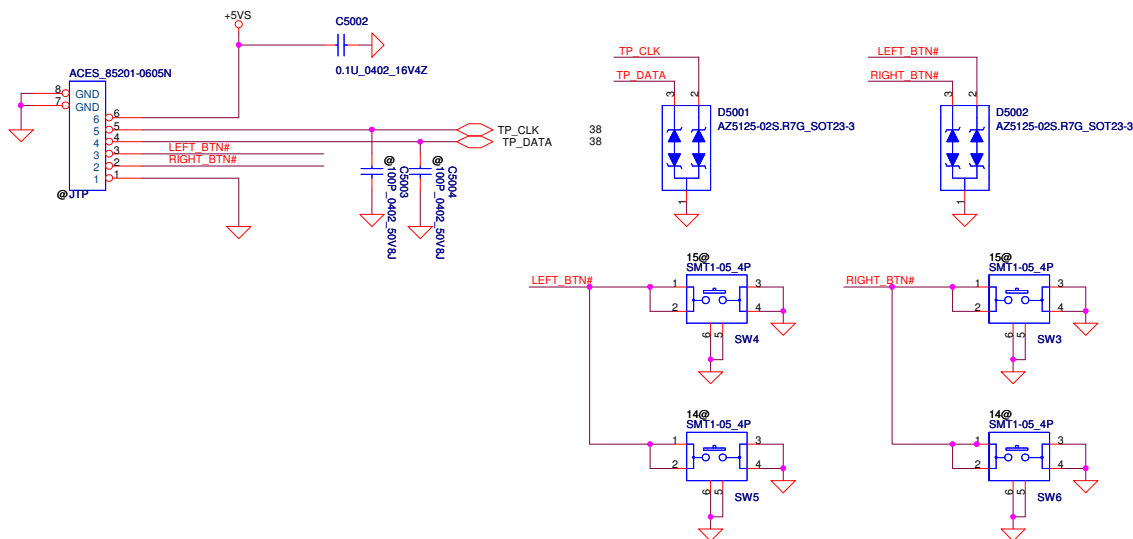
## HEADPHONE OUT JACK



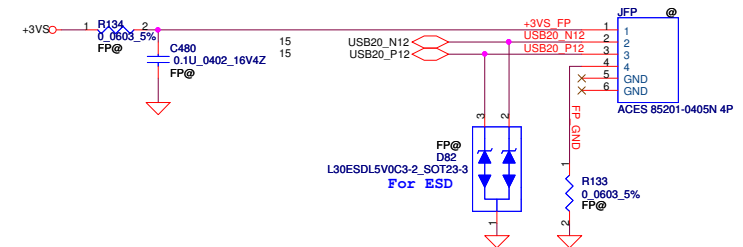
## MICROPHONE IN JACK



## Touch/B Connector

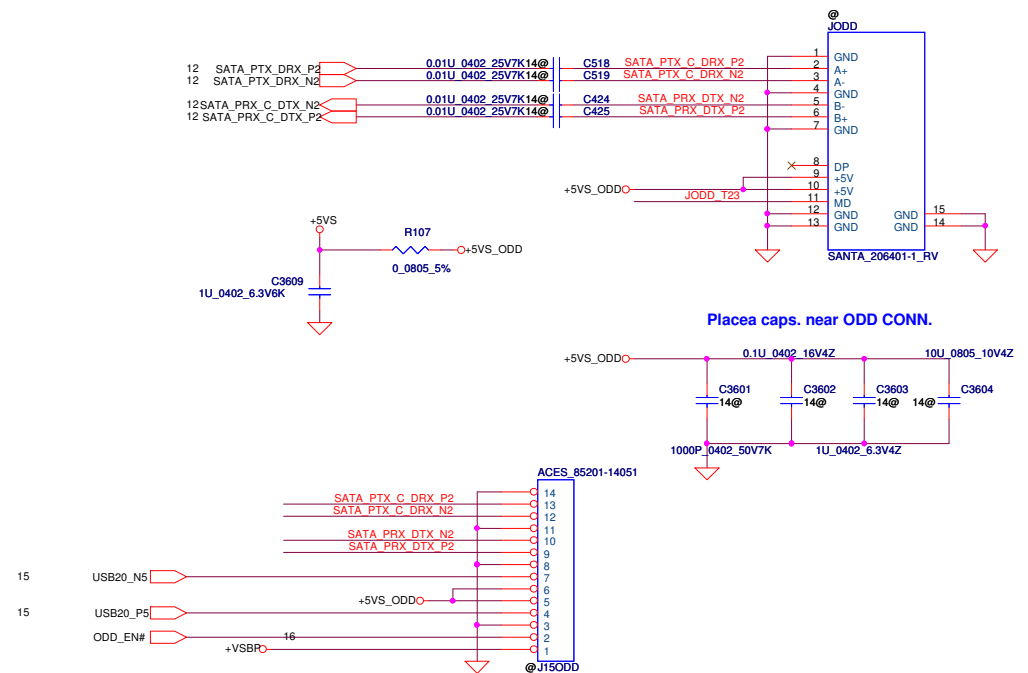
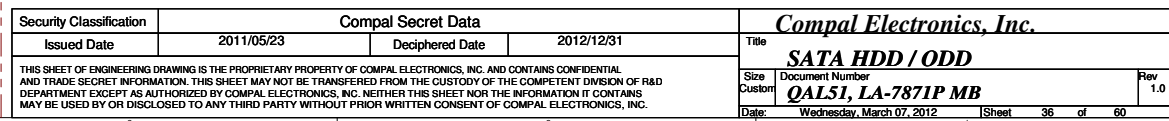


## Finger Printer Connector



Title			
Card Reader RTSS129			
Size	Document Number	QAL51, LA-7871P MB	
Date:	Wednesday, March 07, 2012	Sheet	35 of 60

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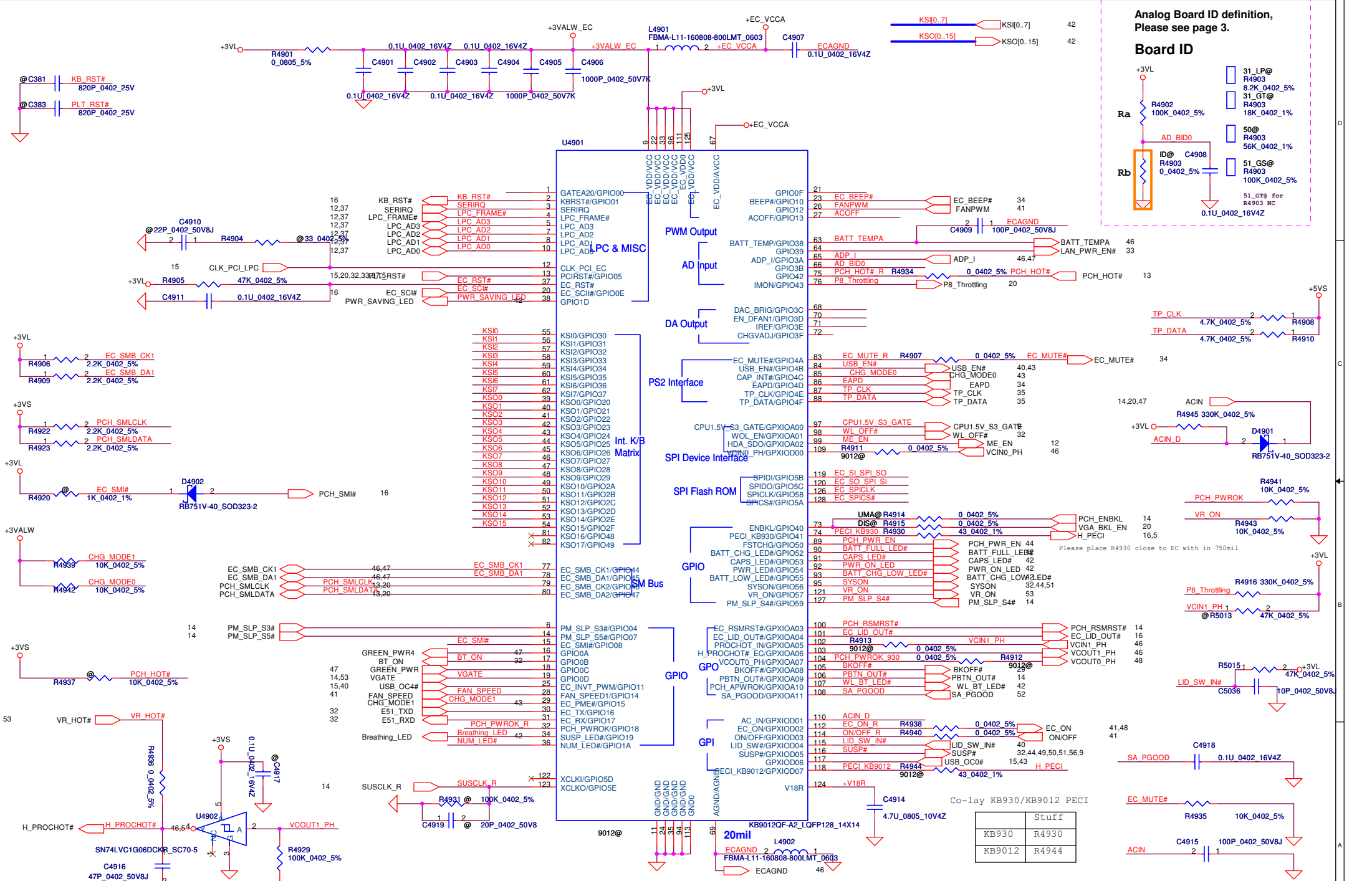


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```
0 = 02Eh
1 = 04Eh
```

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Size	Document Number	Date		Rev	
B	QAL51, LA-7871P MB	Wednesday, March 07, 2012		1.0	
Sheet		38		of	
Page		38		of	

## 4MByte

WIN8@  
R408  
0\_0402\_5%

PCH\_SPI\_CS1#

PCH SPI CS1#  
PCH SPI MISO

R406  
33\_0402\_5%

WIN8@

U60 WIN8@

CS#  
SO  
WP#  
GND

VCC  
HOLD#  
SCLK  
SI

MX25L1606EM21-12G\_S08

PCH SPI CLK WIN8  
PCH SPI MOSI WIN8

R405  
33\_0402\_5%

WIN8@

R404  
33\_0402\_5%

WIN8@

C406  
0.1U\_0402\_16V4Z

WIN8@

+3VS

For EMI reserbt.

@C362 @R420

6P\_0402\_25V 10\_0402\_5%

PCH SPI CLK WIN8

C403  
12P\_0402\_50V8J

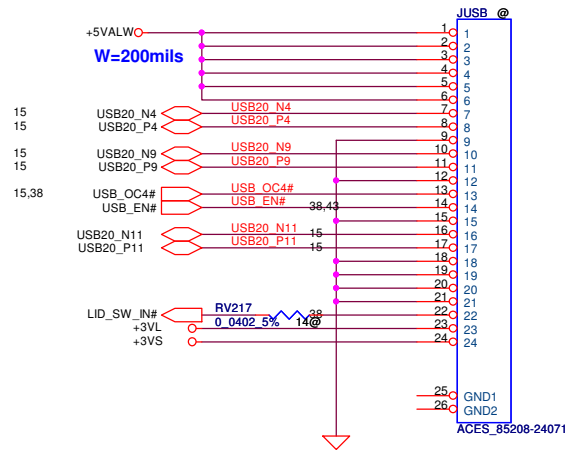
WIN8@

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				Size <b>QAL51, LA-7871P MB</b>	Rev <b>1.0</b>
Date: <b>Wednesday, March 07, 2012</b>				Sheet <b>39</b> of <b>60</b>	

USB + Audio SB

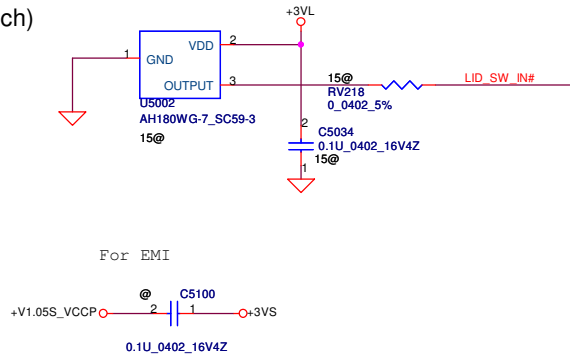
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK



Lid Switch

(Hall Effect Switch)

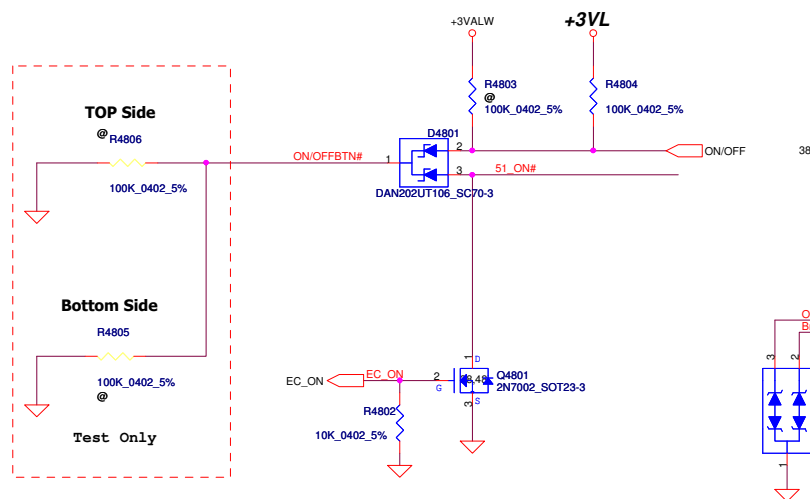


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				Function Board	
				Size	Document Number
				QAL51, LA-7871P MB	
				Date:	Wednesday, March 07, 2012
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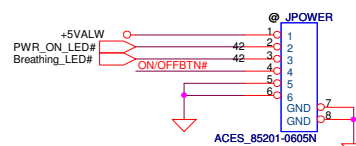


## Power Button

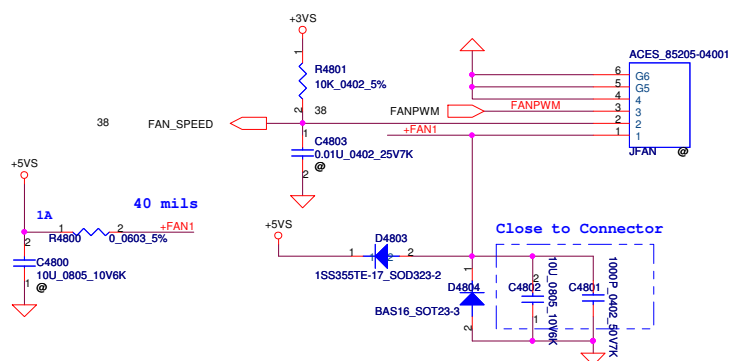
ON/OFF switch



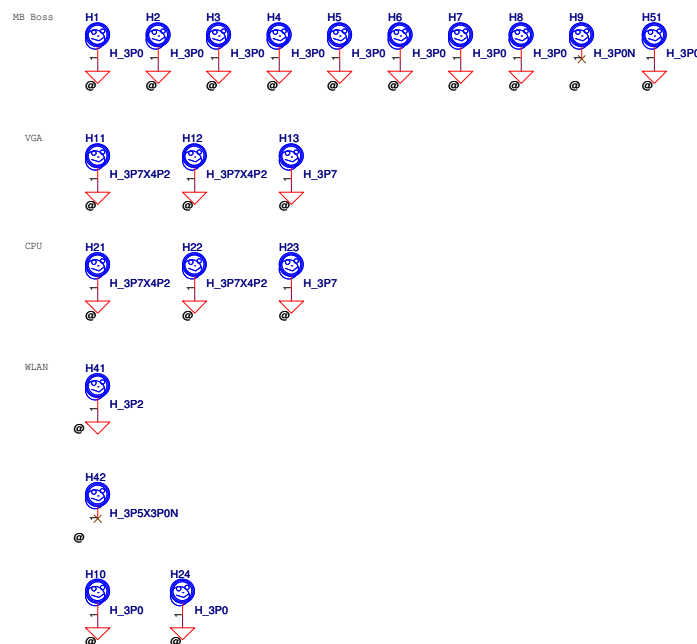
***To POWER/B***



## Fan Control Circuit



## Screw Hole

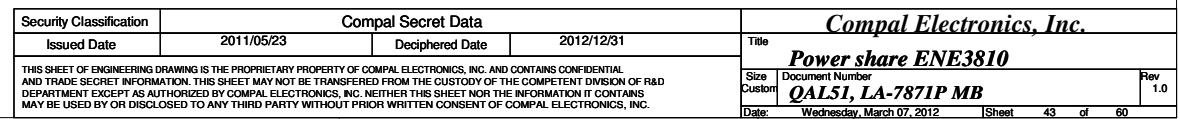


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				Date:	Wednesday, March 07, 2012	Sheet 41 of 60

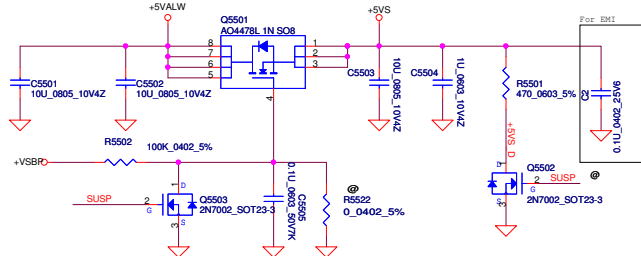
## SATA



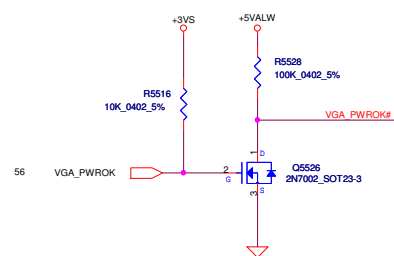
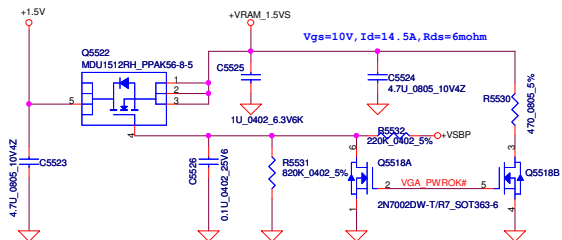
USB3.0 Port0  
Port 0 : Left USB3.0



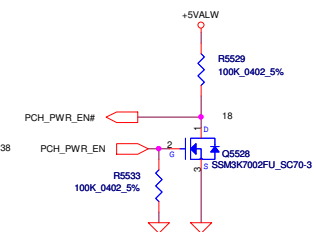
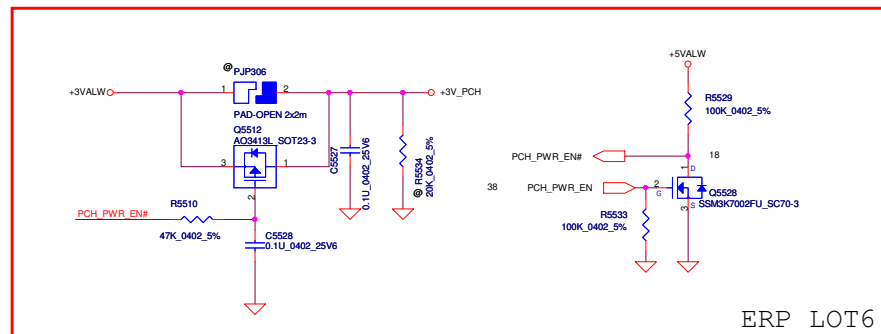
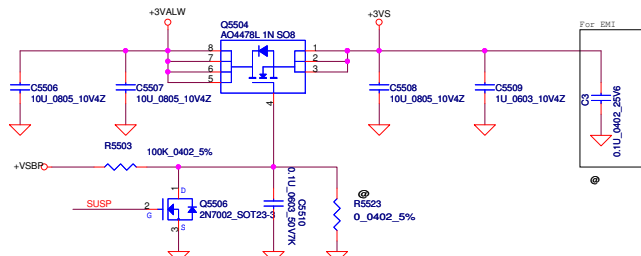
# +5VALW to +5VS



# +1.5V to +VRAM\_1.5VS



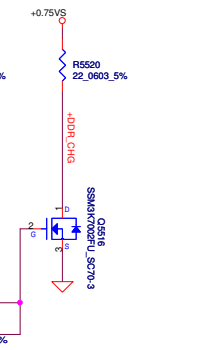
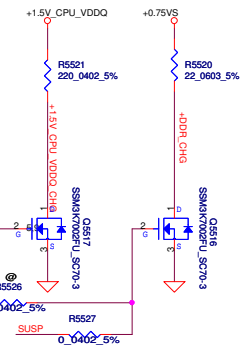
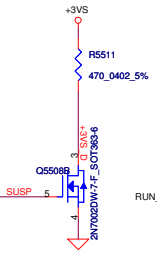
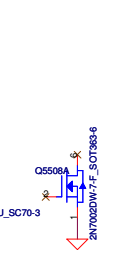
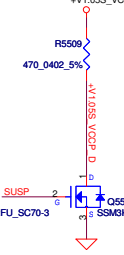
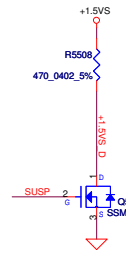
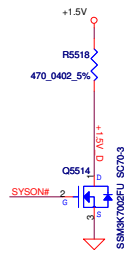
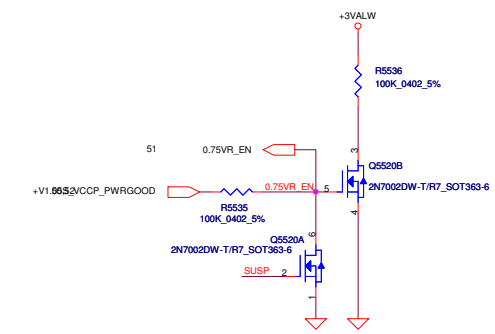
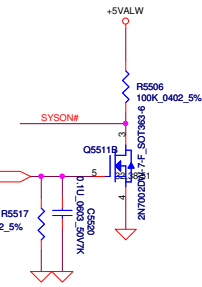
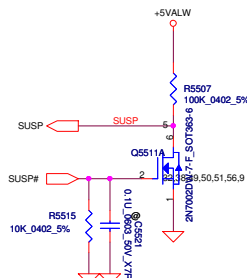
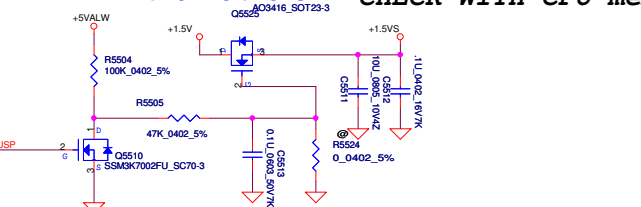
# +3VALW to +3VS



ERP LOT6

# +1.5V To +1.5VS

CHECK WITH CPU memory power



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